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MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

FIFTH SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION
NOV/DEC 2015
SUBJECT: VLSI DESIGN [ECE 305]

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ANY FIVE** full questions.
- Missing data may be suitably assumed.

1A. Derive the expression for drain current I_{DS} for MOSFET in saturation region.

1B. In a CMOS inverter given that V_{thn} = 0.83 V, V_{thp} = - 0.9 V, V_{dd} = 5 V. Find the value of logic threshold V_{inv} for following cases : [i] $\beta_n = 0.4\beta_p$ [ii] $\beta_n = 2.5\beta_p$

1C. What is the pull-up to pull-down ratio for the depletion load NMOS inverter INV2 driven by another similar depletion load NMOS inverter INV1 for the cases shown in FIG Q1(C)? Give your comments

(5+3+2)

2A. [i] Give a transistor-level schematic circuit for a CMOS logic gate for following functions: (a) $Y = \overline{A.(B+C)+D}$ (b) $Y = \overline{AB+CD}$ (c) $Y = \overline{(A \odot B)}$
(d) $Y = \overline{(A+B).(C+D)}$
[ii] With a schematic circuit explain the working of Tri-state inverter.

2B. Explain why NMOS and PMOS pass transistor is not preferred over transmission gate. Give implementation of 3-input XOR gate with minimum number of transmission gates. Input signals A, B, C and its compliments are available.

2C. Give the implementation of $Z = A + B.(C + D)$ using pseudo-NMOS logic design style

(5+3+2)

3A. With the help of neat diagrams explain the fabrication of CMOS inverter using SOI process. State any two advantages of SOI process over traditional CMOS.

3B. Draw the layout for following:
[i] Metal2-to-diffusion connection using via and cut
[ii] Contact from metal2-to-metal1 and then to other layer
[iii] Buried contact with connecting layers

3C. Draw the stick notation and layout for NMOS pass transistor based implementation of 2:1 MUX with enable control input. (5+3+2)

4A. Find the optimal number of NMOS inverters to be cascaded so as to drive load capacitance of 1.48 pF off-chip capacitive load such that the total delay is minimized. Given that 1square C_g = 0.01 pF. Give the cascaded structure showing L: W ratios. Find the overall delay T_d showing the delay across each inverter stage.

4B. Define static power dissipation P_s. Compare static power dissipation in a depletion-mode NMOS inverter and Pseudo-NMOS inverter with justification.

4C. State the different components of power dissipation in a CMOS circuit.

(5+3+2)

5A. Give the circuit implementation of following multiple output SOP function using a Depletion-NMOS based PLA. Give the stick notation.

$Z_1 = \overline{A}\,\overline{B}\,C + \overline{B}\,C$; $Z_2 = \overline{A}\,\overline{B}\,C$; $Z_3 = A\,B\,C + \overline{B}\,C$

5B. With a truth table, give the NMOS gate based implementation of SR latch using only NOR gates.

5C. Identify the MOS based circuit structure given in FIG. 5(C) and explain the function implemented by the circuit.

(5+3+2)

6A. Explain the concept of leaf cell and structured design approach as applied to implementation of N-bit bus arbitration logic.

6B. Bring out differences between constant E field and constant voltage scaling. Discuss scaling effect of these models on following parameters: [i] Gate oxide capacitance C_g [ii] Drain-to-source saturation current I_{dss}.

6C. Refer the pass-transistor based logic network given in FIG 6C.
[a] Determine the truth table for the circuit. What logic function does it implement?
[b] Does the PMOS transistor serve any useful purpose?

(5+3+2)

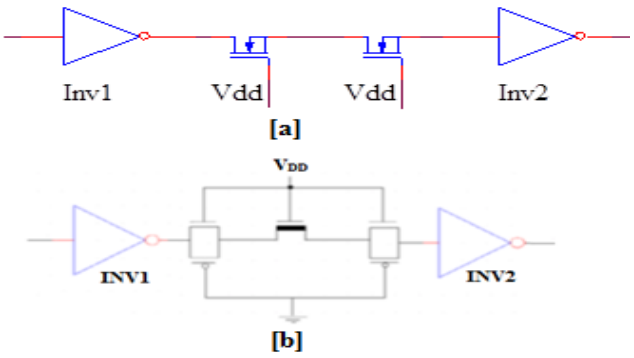

FIG Q1(C)

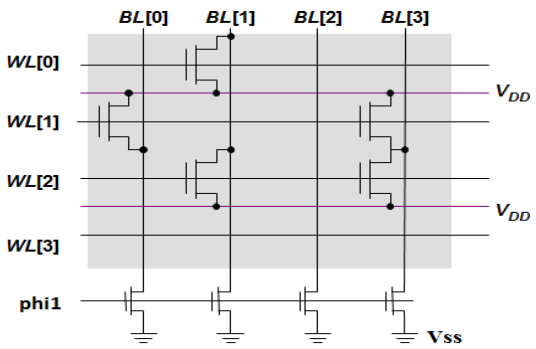

FIG Q5 (C)

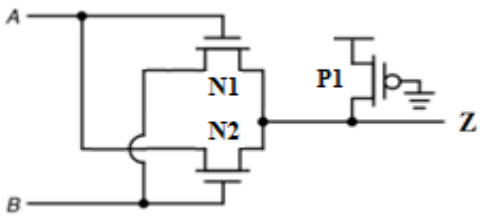

FIG 6(C)