Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY, MANIPAL 576104

(Constituent College of Manipal University)

FIFTH SEMESTER B.TECH (IT) DEGREE END SEMESTER EXAMINATION, NOV/DEC 2015
SUBJECT: EMBEDDED SYSTEMS (ICT 303)
(REVISED CREDIT SYSTEM)

TIME: 3 HOURS **27 /11/2015** **MAX. MARKS: 50**

Instructions to candidates

- Answer any **FIVE FULL** questions.
- Missing data, if any, may be suitably assumed.

1A. Explain the following 8051 instructions with an example to each:
i) DA A ii) MOVX iii) SWAP iv) CJNE v) JBC

1B. What is "Priority Inversion"? Explain how NPCS protocol overcomes this.

1C. Explain the priority of interrupts in 8051.Assume that after RESET, the interrupt priority is set by instruction MOV IP, #00001010B. Discuss the sequence in which interrupts are serviced.

[5+3+2]

2A. Given the following set of periodic tasks:
$T_1 = (3, 0.5)$, $T_2 = (4, 2.5)$, $T_3 = (6, 1)$.
Verify the schedulability of these tasks on a single processor according to the LST algorithm.

2B. With the aid of a neat diagram explain how 3 × 3 matrix keyboard can be interfaced to 8051.Write an 8051 assembly language function which scans the keyboard for a key press and returns the key code.

2C. Bring out the differences between:
i) DC motor and stepper motor
ii) interrupt and polling

[5+3+2]

3A. Explain how an ADC 0804 can be interfaced to the 8051.Write an 8051 assembly language program to monitor INTR pin and bring an analog input into register B.

3B. Assume that with the pin P2.2 connected to pin P3.2, 8051 is RESET and the following error free program is executed; What is the frequency of the square waveform on pin P2.1? Justify. (Assume XTAL= 12 MHz)

```
        ORG 0
        LJMP MAIN
        ORG 3
        CPL P2.1
        RETI
        ORG 13
        CPL P2.2
        RETI
        ORG 30H
MAIN:   SETB P3.2
        SETB TCON.0
        MOV TMOD,#02
        MOV IE,#81H
        MOV TH0,#0
 UP:    SETB TR0
HERE:   JNB TF0,HERE
        CLR TF0
        CPL P2.2
        SJMP UP
```

3C. List and explain the characteristics of commercially available Real Time Operating Systems.

[5+3+2]

4A. Write an 8051 C program to transfer the message "Inspired by Life" serially, repeatedly at 57,600 baud rate. Assume serial mode-1.(XTAL = 11.0592 MHz)

4B. Define "Addressing mode". With suitable examples, explain any four addressing modes available in 8051.

4C. Define "Hyper period". Mention its importance in static scheduling.

[5+3+2]

5A. Interface a single 2 MB NV-RAM chip to 8051. Show the necessary connection. Write an 8051 C program to transfer an array of 200 bytes from source block (starting address 01FF9BH) to a destination block (starting address 12FF9BH) of this memory. Explain various steps involved in performing READ/WRITE operation with respect to this memory.

5B. Discuss the scheduling, allocation and priority inheritance rules of the basic Priority Ceiling Protocol.

5C. Write single 8051 instruction for each of the following:

(i) To select Bank-2 as active bank

(ii) To disable all interrupts

[5+3+2]

6A. Assuming that a switch is connected to pin P3.3 of 8051 and common cathode 7 segment displays are connected to P2 and P1, write an 8051 C program using interrupts to display number of times the switch connected to P3.3 is pressed on 7 segment displays (in BCD) while producing a square wave of frequency 200 KHz on P0.3.

6B. With a neat diagram, explain the functional pin diagram of 8051.

6C. Define "UART". What is its role in serial communication?

[5+3+2]