Reg. No.										

Manipal Institute of Technology, Manipal

(A Constituent Institute of Manipal University)

FIFTH SEMESTER B.TECH (INSTRUMENTATION & CONTROL ENGINEERING)

END SEMESTER EXAMINATIONS, NOV/DEC 2015

SUBJECT: DIGITAL SYSTEM DESIGN [ICE 311]

Time: 3 Hours MAX. MARKS: 50

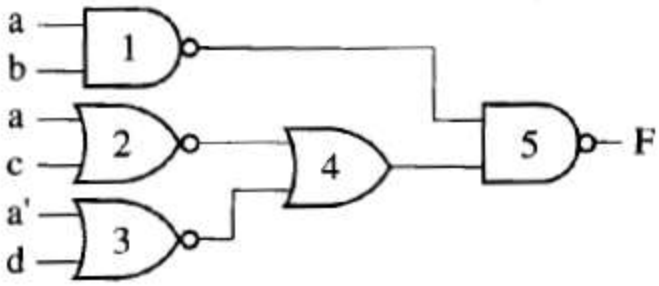
Instructions to Candidates:

- Answer **ANY FIVE FULL** questions.
- Missing data may be suitably assumed.

1A. Write the truth table for the following equation: **2**

$$F = (A \oplus B)C + A'(B \oplus C)$$

1B. Find all the static-1 hazards in the following network: **4**



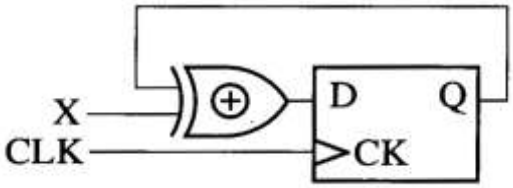
Design a NAND-gate network that is free of the hazards.

1C. Design a Moore sequence detector to detect the sequence "0110".Draw the state graph and state table for this Moore machine. **4**

2A. A D flip-flop has a setup time of 4 ns, a hold time of 2 ns, and a propagation delay from the rising edge of the clock to the change in flip-flop output in the range of 6 to 12 ns. The XOR gate delay is in the range of 1 to 8 ns. **3**

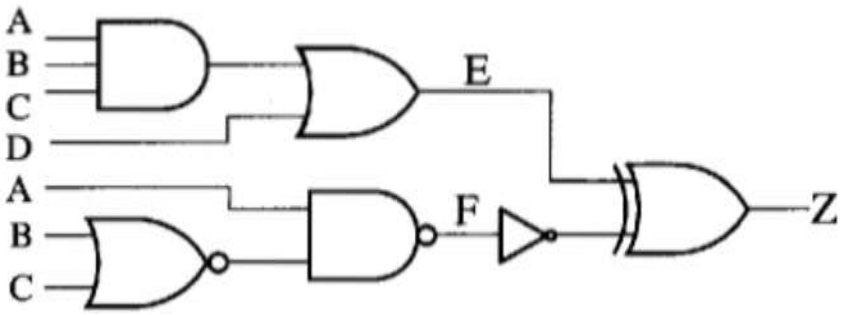
(a) What is the minimum clock period for proper operation of the following network?

(b) What is the earliest time after the rising clock edge that X is allowed to change?



2B. Explain the structure of a VHDL program. **3**

2C. Write a VHDL description of the following combinational circuit using concurrent **4**



statements.

3A. Write a behavioral VHDL code for a D flip-flop. **3**

3B. Develop a full adder with appropriate truth table and circuit elements. Assuming components write a structural code. **4**

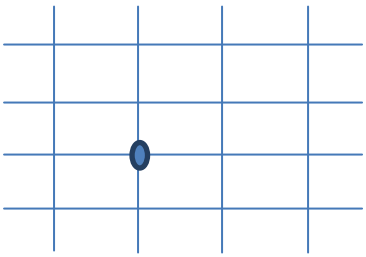
3C. (a) Show that the functions F1 and F2 are the same using Boolean algebra. **3**

$$F1 = (X + \bar{Y})Z + \bar{X}Y\bar{Z}$$

$$F2 = (X + \bar{Y} + \bar{Z})(\bar{X} + Z)(Y + Z)$$

(b) Develop full VHDL code for function F2.

4A. Show iterations for keypress: **4**



4B. With signal declaration examples, explain the std_logic, std_logic_vector and integer datatypes. **2**

4C. What are the different control structures discussed in the keypad scanner system? Describe the working of anyone with a code snippet from the keypad scanner system. **4**

5A. For a 5 MHz clock, with appropriate signal declarations, write a VHDL program to generate a single cycle done signal at the end of 100 μs. **3**

5B. Briefly explain how ROMs are classified. **3**

5C. Explain the different types of FPGA programming technologies. **4**

6A. Implement the following state table using a ROM and D flip-flops. **4**

Present state	Next state		Output (Z)	
	X=0	X=1	X=0	X=1
S0	S0	S1	0	1
S1	S2	S3	1	0
S2	S1	S3	1	0
S3	S3	S2	0	1

6B. Explain how testing of combinational circuits is performed along with different types of faults encountered. **3**

6C. Explain scan testing with a block diagram. **3**