Reg. No.										

Manipal Institute of Technology, Manipal

(A Constituent Institute of Manipal University)

FIFTH SEMESTER B.TECH (INSTRUMENTATION & CONTROL ENGINEERING)

END SEMESTER EXAMINATIONS, NOV/DEC 2015

SUBJECT: DIGITAL SYSTEM DESIGN [ICE 311]

Time: 3 Hours MAX. MARKS: 50

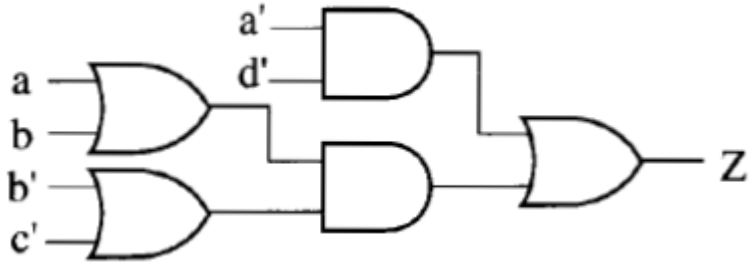
Instructions to Candidates:

- Answer **ANY FIVE FULL** questions.
- Missing data may be suitably assumed.

1A. Determine the prime-implicants of the function: **3**

$$F(w,x,y,z) = \sum(1,4,6,7,8,9,10,11,15)$$

1B. Find the static-0 hazards in the following circuit. **3**



Redesign the circuit so that it is free of static hazards. Use gates with at most three inputs.

1C. For the input and output sequence given below: **4**

Input=1010110101010

Output=0001000010101

Draw Mealy state graph and state table.

2A. Consider the following digital device in Fig. 2A. The timing characteristics of its components are available in the table below. What are the timing characteristics of the overall device? Calculate the setup time and the minimum clock period for proper operation of the circuit. **3**

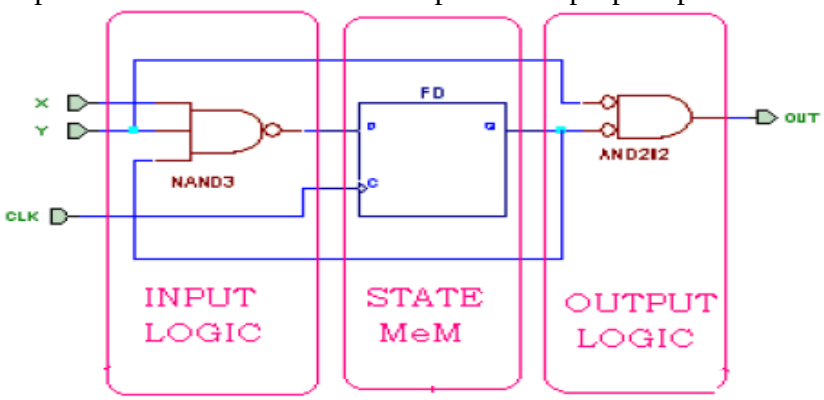


Fig. 2A

Device	Propagation Delay (Minimum)	Propagation Delay (Maximum)	Setup Time	Hold Time
D Flip Flop	4 ns	8 ns	10 ns	3 ns
NAND Gate	3 ns	6 ns	X	X
Bubbled AND Gate	2 ns	4 ns	X	X

2B. Draw a complete Y-chart showing different levels and domains of abstraction. **3**

2C. (a) Write VHDL code for a full adder using logic equations. **4**
(b) Write structural VHDL code for a 4-bit full adder using module defined in (a) as a component.

3A. Consider the following VHDL code: **3**

```
entity Q3 is
port(A,B,C,F,Clk:in bit;
     E:out bit);
end Q3;
architecture Qint of Q3 is
signal D,G:bit;
begin
process(clk)
begin
if clk'event and clk='1' then
D<=A and B and C;
G<=not A and not B;
E<=D or G or F;
end if;
end process;
end Qint;
```

(a) Draw a block diagram for the circuit. (at block level)
(b) Give the circuit generated by the preceding code. (at gate level)

3B. For the state table shown below, write full behavioral code: **4**

Present state	Next state		Output
	X=0	X=1	
S0	S1	S0	00
S1	S0	S2	01
S2	S2	S1	10

3C. Explain working of a 4×4 keypad scanner using a flowchart. **3**

4A. Explain case statements using example of column scanning logic. **4**

4B. For a 10 MHz clock and active low reset, generate a single o_done signal at the end of 100 µs. Counter is operational only when i_counter_start is high. Write a VHDL code (signal declarations & process only) and the timing diagram for the above. **4**

4C. Briefly explain the different operators used in VHDL. **2**

5A. Write a test bench to verify the working of a JK flip-flop. **4**

5B. Implement the following state table using ROM and flip-flops and illustrate the design using a truth table and block diagram. **3**

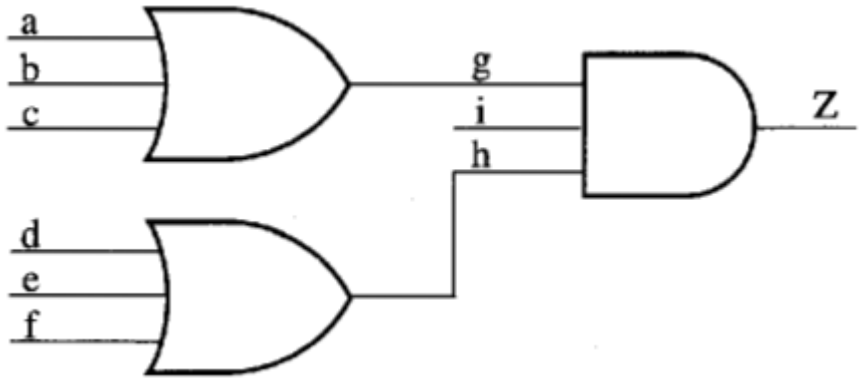
Present state	Next state		Output	
	X=0	X=1	X=0	X=1
S0	S1	S0	0	0
S1	S2	S0	0	0
S2	S4	S3	0	0
S3	S1	S0	1	0
S4	S4	S0	0	0

5C. Find a minimum-row PLA to implement the following three functions: **3**

$$f(A,B,C,D) = \Sigma m(3,6,7,11,15)$$
$$g(A,B,C,D) = \Sigma m(1,3,4,7,9,13)$$

6A. With diagrams explain the different types of FPGA architectures. **4**

6B. Find the minimum set of tests that will test all stuck-at-1 faults in the following circuit. For each test, specify the faults tested. **3**



6C. Explain boundary scan testing with a neat diagram. **3**

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