Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

FIFTH SEMESTER B.Tech. (MECHATRONICS) DEGREE END SEMESTER EXAMINATION
December 2015 /January 2016
SUBJECT: FPGA BASED DIGITAL SYSTEM DESIGN (EC 357)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ANY FIVE** full questions.
- Missing data may be suitably assumed.

1A.	List and explain the advantages of integration.	
1B.	Write a Verilog HDL program to using data flow modelling for a 1:4 Demultiplexer.	
		(5+5)
2A.	Show the gate level modelling of a NAND gate and write the test bench for the same.	
2B.	With suitable examples explain how constants are declared and used in Verilog HDL.	
		(5+5)
3A.	Design a circuit using PAL for the expression given in Q3A.	
3B.	Describe at least 3 differences between the Xilinx XC 3020 and Xilinx 4000 series CLB using suitable diagrams.	
		(5+5)
4A.	Realize a full adder using a PLA.	
4B.	Describe, with the help of a diagram, the I/O block of the Xilinx XC 3020 logic cell array.	
		(5+5)
5A.	Explain the various ways of detection of faults in a logic circuit with suitable examples.	
5B.	Find the test vector/s for s-a-0 fault at ‘a’, in the circuit of Q5B using Boolean Difference Method.	
		(5+5)
6A.	With a suitable example describe how transition count testing is superior to random testing of sequential circuits.	
6B.	Find the homing sequence for the state diagram shown in Q6B.	
		(5+5)

w (a, b, c, d) = ab’ + c’d’ + abcd
x (a, b, c, d) = a’b’c’d’ + cd
y (a, b, c, d) = ab + bc + ac
z (a, b, c, d) = a + b + c

Expression Q 3A

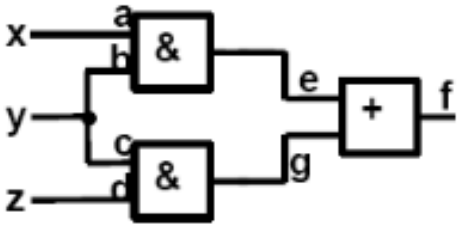

Figure Q 5B

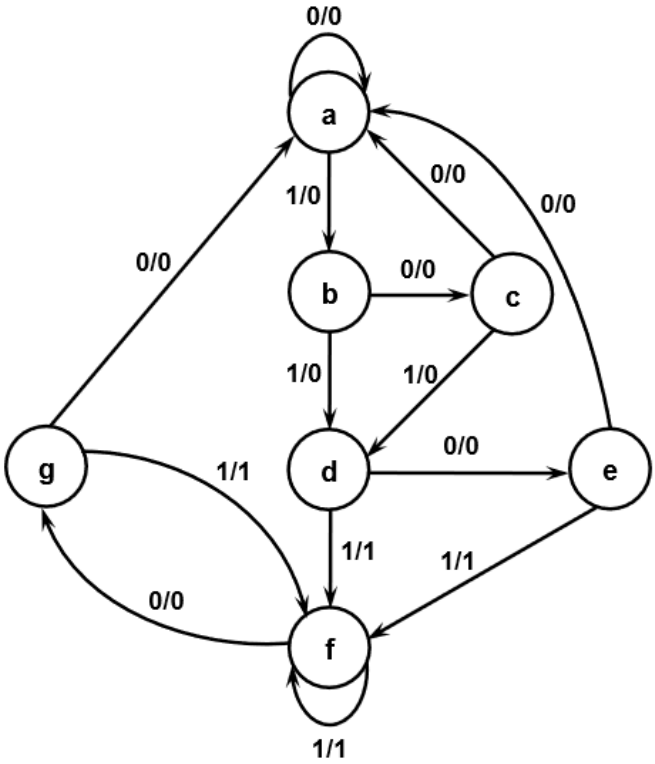

Figure Q 6B