Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

FIFTH SEMESTER B.Tech. (MECHATRONICS) DEGREE END SEMESTER EXAMINATION
November /December 2015
SUBJECT: FPGA BASED DIGITAL SYSTEM DESIGN (EC 357)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ANY FIVE** full questions.
- Missing data may be suitably assumed.

1A.	Describe the various digital system design methodologies in detail.	
1B.	Write a program for the behavioural model of a Serial in Parallel Out shift register using Verilog HDL.	
		(5+5)
2A.	Code the circuit in Q 2A using gate level modelling in Verilog HDL.	
2B.	With suitable examples explain the various compiler directives that are available with Verilog HDL.	
		(5+5)
3A.	Design a ROM for a BCD to 7-segment display converter.	
3B.	With suitable diagrams explain the various combinational logic options available with the Xilinx XC 3020 logic cell array.	
		(5+5)
4A.	Realize a 3:8 decoder using a PLA.	
4B.	Illustrate and explain the difference between shareable and parallel expanders in the Altera 7000 series FPGA.	
		(5+5)
5A.	With the input test vector 110, perform Parallel Fault simulation for the circuit shown in Q5A.	
5B.	Find the test vector for the circuit in Q5B for a s-a-0 fault at ‘d’ using D algorithm.	
		(5+5)
6A.	Determine the faults that can be detected in the circuit in Q6A for the input test vector {10010} using Deductive Fault Simulation method.	
6B.	For the 4 bit signature generator shown in Q6B perform signature analysis for the output sequence generated from the tested circuit as 10011. Draw an inference whether the tested circuit is faulty or not, assuming that the perfect version of the tested circuit has a signature of 0100. At start up assume the contents of the register to be 0000.	
		(5+5)

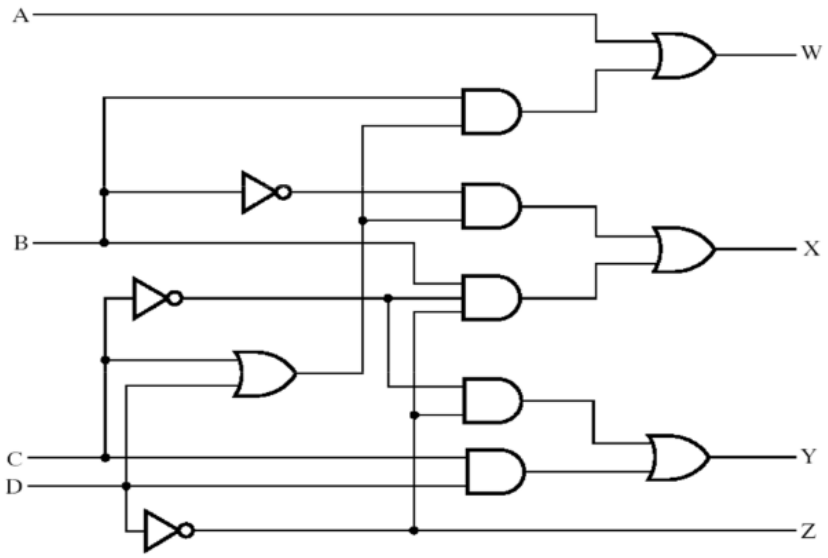

Figure Q 2A

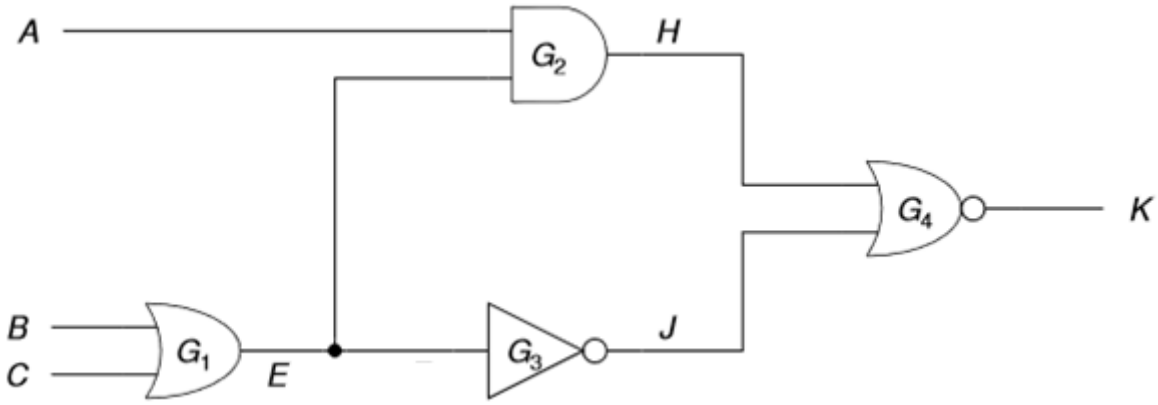

Figure Q 5A

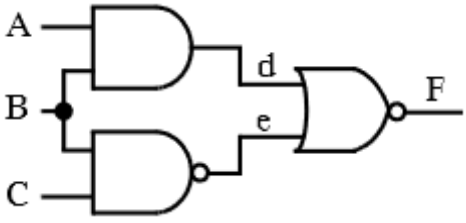

Figure Q 5B

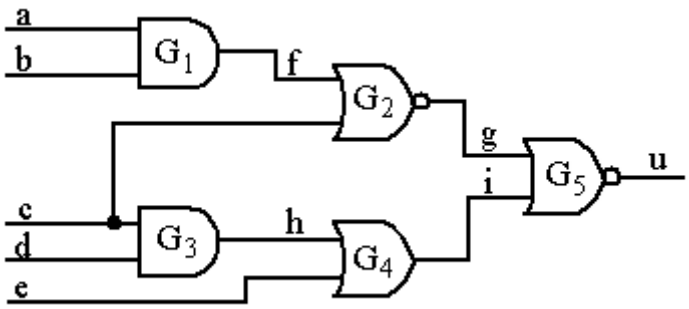

Figure Q 6A

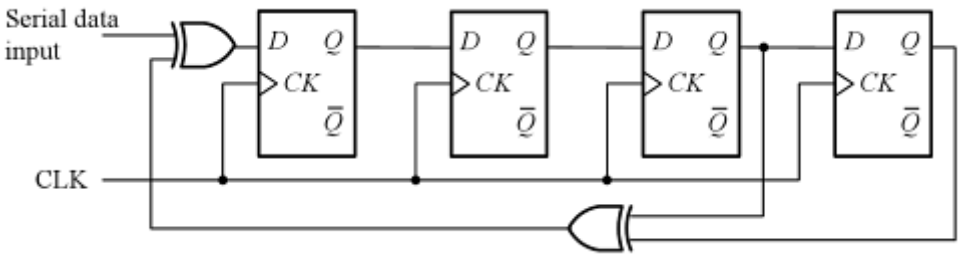

Figure Q 6B