Reg. No.										

Manipal Institute of Technology, Manipal

(A Constituent Institute of Manipal University)

VII SEMESTER B.TECH (MECHATRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, NOV/DEC 2015

SUBJECT: ADVANCED EMBEDDED SYSTEM DESIGN [ECE 453]

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ANY FIVE FULL** the questions.
- Missing data may be suitably assumed.

1A Draw the programming model of ARM processor and explain the following:
(i) Load-store architecture. (ii) Conditional execution. (iii) Register file.

1B Differentiate between the following:
(i) ARM modes of operation (ii) ARM states.

1C Write the instruction format of ARM data processing instruction. (5+3+2)

2A Write a program to find the sum of 10 numbers in an array. The array is stored in memory location 23000000h. Store the result in memory location 32000000h.

2B Given r0=10000000h and r2=04h. Identify the addressing mode of the following instructions. Write the contents of r1 and r0 registers after the instruction is executed in each case.
(i) LDR r1, [r0, r2]! (ii) LDR r1, [r0, #0x08] (iii) LDR r1, [r0], r2, LSR #0x2

2C Explain the following assembler directives with an example for each.
(i) DCW (ii) AREA (5+3+2)

3A Assume a switch to be connected to the pin P1.0 of the processor, a common cathode 7-segment display to P3.0 to P3.7 and 4 LEDs to P2.0, P2.1, P2.2 and P2.3 of the processor. Write a program to display “1” on the 7-segment display and display MOD-8 up counter on the LEDs when the switch is pressed else display “0” on the 7-segment display and display MOD-8 down counter on the LEDs. Assume switch bounce period is 0ms.

3B List out the steps taken by the ARM processor when an exception occurs.

3C Write the 3-stage pipeline (as per ARM7) execution flow of the following sequence of instructions till 11 clock cycles.

```
MOV r2,#8
ADD r1,r3,r3,LSL #1
B L2
SUBS r4,r4,r2
EORS r1,r3,r4
MOV r2,#5
L1: B L1
```

```
L2: MUL r3,r2,r2
STR r3,[r0]
ANDS r5,r3,r0
MOV PC, LR
END
```
(5+3+2)

4A Given r3=0x02 and r5=0x0C. What would be the contents in registers in each of the following cases after the Thumb instruction is executed.

(i) SUB r5,r3
(ii) CMP r5,r3
(iii) MVN r5,r3
(iv) NEG r5,r3
(v) AND r5,r3
(vi) TST r3,r5
(vii) LSL r5,r3
(viii) LSR r5,r3
(ix) EOR r5,r3
(x) ROR r5,r3

4B Write the syntax and explain the following Thumb instructions.
(i) Multiple register load-store instructions.
(ii) Stack instructions (iii) Software interrupt instruction

4C Draw the Thumb programmer's model. List out the differences between ARM and Thumb instruction sets. (5+3+2)

5A Explain with an example, how Thumb instruction is mapped to ARM instruction.

5B With a neat diagram, show the relationship a cache has between main memory and processor core.

5C The access time of a cache memory is 60ns and that of the main memory is 600ns. It is estimated that 80% of the main memory requests are for read and the remaining are for write. The hit ratio for read access only is 0.9 and a write through policy is used. Determine the average access time considering only the read cycles. What is the average time if the write requests are also taken into consideration. (5+3+2)

6A Explain the following terms briefly -
(i) Overlapping and background regions.
(ii) Cache mapping techniques
(iii) MPU and MMU.
(iv) Cache replacement policies.
(v) Cache write policies.

6B Draw the internal architecture of VLSI Ruby II Advanced communication processor and list out its salient features. (5+5)