Reg. No.										

Manipal Institute of Technology, Manipal

(A Constituent Institute of Manipal University)

VII SEMESTER B.TECH (MECHATRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, DEC/JAN 2016

SUBJECT: ADVANCED EMBEDDED SYSTEM DESIGN [ECE 453]

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ANY FIVE FULL** the questions.
- Missing data may be suitably assumed.

1A With a neat diagram, explain the programming model of ARM processor.

1B Differentiate between the following:
(i) ARM modes of operation (ii) ARM states.

1C Write the CPSR format and explain the significance of each bit. (5+3+2)

2A Write a program to find the least number in an array of 10 numbers. The array is stored in memory location 23000000h. Store the result in memory location 32000000h.

2B Explain the addressing modes used in ARM programming.

2C Explain the following assembler directives with an example for each.
(i) RN (ii) EQU (5+3+2)

3A Explain the following opcodes of ARM instruction set.
(i) RSB (ii) SWP (iii) TST (iv) BL (v) MRS

3B Explain ARM exceptions briefly.

3C Explain the ARM 3-stage pipeline employed in ARM 7 processor. (5+3+2)

4A List out the similarities and differences between ARM and Thumb instruction sets.

4B Draw the Thumb programmer's model. List the properties of Thumb code.

4C Write the syntax and explain the following Thumb instructions.
(i) Multiple register load-store instructions. (ii) Stack instructions (5+3+2)

5A Explain with an example how Thumb instruction is mapped to ARM instruction.

5B Define the following terms.
(i) Logical and physical cache
(ii) Cache hit and cache miss
(iii) Temporal and spatial locality

5C Calculate t', Y and A of a memory system whose parameters are indicated as follows: t_c=160ns, t_m=960ns,h=0.9. (5+3+2)

6A Explain the following terms briefly -
(i) Protected and unprotected systems.
(ii) Cache mapping techniques
(iii) MPU and MMU.
(iv) Cache allocation policies.

(v) Cache write policies.

6B Draw the internal architecture of VLSI Ruby II Advanced communication processor and list out its salient features. (5+5)