Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

I SEMESTER M.TECH. (COMPUTER SCIENCE AND ENGINEERING)

END SEMESTER EXAMINATIONS, NOV/DEC 2016

SUBJECT: HIGH PERFORMANCE COMPUTING SYSTEMS [CSE 5104]

REVISED CREDIT SYSTEM
(01/12/2016)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** questions.
- Missing data may be suitable assumed.

1A. Starting from CPU time, derive the processor performance equation to calculate CPI that uses individual CPI and the fraction of occurrences of that instruction in a program. **3M**

1B. Starting from basic principles, discuss the classification of parallel computer based on degree of parallelism. **4M**

1C. Give the complete detailed configurations of Columbia Supercomputer. **3M**

2A. Write a detailed note on models for communication and memory architecture in multiprocessor systems. **3M**

2B. What do you mean by cache coherence protocol? Illustrate the invalidation protocol working on a snooping bus for a single cache block X with write-back caches. Assume initially the cache is empty and location X has the value 0. **3M**

2C. Write an MPI program to add elements of an array using two processes. Use the user friendly statements wherever it is needed. **4M**

3A. Draw a neat diagram showing the basic structure of a Tomasulo-based processor, including both the FP-unit and the load-store unit. Explain the functionality of each of them. Also discuss the various fields of Reservation Station. **4M**

3B. Write a summary note on Loop Unrolling and Scheduling. **3M**

3C. Discuss the two important properties that lead on usage of Reservation stations, instead of register file. **3M**

4A. Applying a convolution filter to a source image, discuss the sequential code for convolution algorithm. Write the convolution kernel in OpenCL for the same. **4M**

4B. Give a detailed note on OpenCL specification. **4M**

4C. What is heterogeneous computing? What is OpenCL? **2M**

5A. Write a CUDA program for the matrix-matrix addition. In your code handle the matrix elements as one dimensional vector elements. Include cudaStatus verification codes in your program. **4M**

5B. Explain memory hierarchy adopted in CUDA. **3M**

5C. Discuss on threadID, block ID and blockDim with related diagram. **3M**