Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

FIRST SEMESTER M.TECH (DEAC & MICRO) DEGREE
END SEMESTER EXAMINATION - NOV/DEC 2016
SUBJECT: PROCESSOR ARCHITECTURE & APPLICATIONS (ECE – 5103)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. A superscalar pipelined machine, capable of fetching and decoding two instructions at a time, having three functional units (F1 & F2 are 2 integer + F3 is a 1 floating point). Each instruction takes one cycle to execute. Two instances of write back stages.

Given: Ten instruction code segment (I1 to I8)
- I3 and I4 conflict for functional unit F1
- I5 depend on value produced by I4
- I5 and I6 conflict for functional unit F2
- I7 and I8 also conflict for functional unit F2

Implement the above code using **two policies** which take maximum number of clock cycles.

1B. Discuss implementation of 8 tap FIR filter using single, two and eight MAC units with necessary diagrams.

1C. Discuss control hazard in pipelining with an example.

(4+4+2)

2A. Describe an architectural overview, memory system of floating point Digital signal processor.

2B. Discuss the architecture of a processor, which uses memory for all vector operations.

2C. Explain an Interrupt based I/O strategy with algorithm / program used for implementation.

(4+4+2)

3A. Discuss the architecture of a 4 KB cache memory.

3B. With regard to parallel architecture of processors, describe i) SISD ii) SIMD iii) MISD iv) MIMD v) Centralized shared Memory architecture vi) Distributed memory architecture

3C. Analyse role of a write update protocol in a coherent centralized memory based multiprocessor system.

(4+4+2)

4A. Analyse pipelining adopted in Pentium 4.

4B. Build a single cycle data path for implementing combined R –type and memory instructions without pipelining.

4C. A DSP has a circular buffer. Starting address = 0500h and End address = 050Fh. What are the new values of address pointer of buffer if in the course of address computation, it gets updated to i) 0512h b) 04FCh?

(4+4+2)

5A. Write programming model/architecture of mixed signal microcontroller with one application.

5B. Compare Direct mapped cache and set associative cache with necessary examples and diagrams.

5C. Discuss how output of one pipeline is directly released into another pipeline for an equation KX + Y (where K is a scalar constant and X & Y are vectors)

(4+4+2)