Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

FIRST SEMESTER M.TECH (Microelectronics) DEGREE END SEMESTER EXAMINATION - NOV/DEC 2016
SUBJECT: ADVANCED DIGITAL VLSI DESIGN (ECE – 5121)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Derive the expression of drain current of a MOSFET in enhancement mode of operation. Indicate how *Ids* changes if non-ideal conditions like i) Channel length modulation and ii) Velocity saturation are taken into considerations.

1B. Estimate the raise time and fall time of a CMOS inverter and establish the condition for obtaining symmetrical operation.

1C. Define the terms i) Sheet Resistance and ii) Standard unit of capacitance. Give their significance in VLSI.

(5+3+2)

2A. Implement F= $\overline{ABC+D}$ using CMOS gate logic. Draw the lay out using Euler path method and estimate the minimum area required.

2B. With the help of neat diagrams explain the fabrication of CMOS inverter using N-Well process. What are its merits and demerits?

(5+5)

3A. With the help of a circuit diagram explain Dynamic CMOS logic. What are limitations of the circuit? Briefly Explain. Also show how to overcome those limitations.

3B. With the help of suitable diagrams explain the terms Clock skew and Jitter. What are the sources of skew and Jitter? Also explain the impact of skew and Jitter on the circuit performance.

3C. Draw the circuit for a function F = $\overline{((A.B.C)+D)}$ using BiCMOS logic.

(5+3+2)

4A. What is meant by general scaling ? Explain. Also illustrate the impact of general scaling on the following parameters: i) Current density ii) Power delay product and iii) Maximum operating frequency assuming that supply voltage and oxide thickness are scaled by $1/\beta$ while, all other parameters are scaled by $1/\alpha$.

4B. With the help of neat diagrams explain H-Tree and Grid type of clock distribution techniques. Also discuss their salient features.

4C. Draw the circuit of a functionally complete CMOS D latch and list its salient features.

(5+3+2)

5A. With the help of a neat circuit diagram explain how reading and writing are accomplished in a 6-T SRAM cell. Also give the salient features of 6-T SRAM.

5B. With the help of suitable circuits, explain various options for implementing dynamic RAMs and compare them. What are the merits and demerits of DRAM?

(5+5)