Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

FIRST SEMESTER M. TECH (ME) DEGREE END SEMESTER EXAMINATION
NOV/DEC 2016
SUBJECT: ADVANCED DIGITAL VLSI DESIGN (ECE – 5121)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Based on the pull up device employed, classify and evaluate the performance of static inverters in VLSI design.

1B. Compare circuit implementation using switch logic and gate logic.

1C. If a chain of ***N*** pass transistors are connected in series, estimate the total delay in terms of delay unit τ. Assume that all the transistors are of feature size.

(5+3+2)

2A. Implement CMOS circuit for the function F= (A.B ((C+D) E))′, i) Draw the CMOS circuit and show the L:W ratios for each transistors for proper operation and ii) Draw the stick diagram by applying Euler's path.

2B. With the help of neat diagrams explain the fabrication of CMOS inverter using SOI process.

2C. Explain Latch up in CMOS.

(5+3+2)

3A. Implement a full adder circuit using Domino Logic.

3B. Estimate the device size ratio for 2-input NAND gate using Pseudo NMOS logic assuming mobility ratio of 2.

3C. Draw the layout of a two input XOR gate using CMOS.

(5+3+2)

4A. What is the problem with single phase clocking? Explain. Discuss the techniques used to overcome the same.

4B. Discuss the implementation of Dynamic latch. How can you implement an edge triggered flip-flop using such latches? Explain with circuit and timing diagrams.

4C. In a certain synchronous sequential circuit, the timing parameters are as follows: t_{cq}=40ps, $t_{pd,logic}$ = 55ps, t_{su} = 30ps and t_{hold} = 20ps, clock skew = 60ps and jitter = 20ps. Calculate the maximum clock frequency that can be applied. (5+3+2)

5A. Show the complete circuit of a 4 x 4 NAND based ROM (including the NOR based decoder) to store data values of 1, 3, 9 and 6. What are its merits and demerits?

5B. With respect to interconnects discuss the following issues:
i) Inductive parasitic ii) Differential signalling and iii) Cross talk

5C. Discuss the salient features of 1T DRAM cell. In a 1 T DRAM, assume that the cell capacitance is 100fF and that of column capacitance is 1pF. Also the column lines are pre-charged to V_{DD} /2. Compute the voltages on the bit lines when reading a '1' and '0' if V_{DD} = 2.5V.

(5+3+2)