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MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

**FIRST SEMESTER M. TECH (DEAC & ME) DEGREE END SEMESTER EXAMINATION- NOV/DEC 2016**

**SUBJECT: ANALOG AND RF VLSI DESIGN (ECE – 5102)**

**TIME: 3 HOURS** **MAX. MARKS: 50**

**Instructions to candidates**

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Discuss how a Gilbert cell is constructed using differential amplifier circuits. Explain how a Gilbert cell can be used as an analog voltage multiplier?

1B. Given that all the transistors in the circuit of FIG. 1B are operated in saturation region. Find the expression for small-signal differential voltage gain for the circuit shown neglecting channel length effect.

1C. For the circuit shown in FIG. 1C given that $V_{DD}$ = 3 V, $V_{TH}$ = 0.6 V, $(W/L)_{1,2} = 25/0.5$ , $K_n$= 50 $\mu A/V^2$. Assume $\lambda = \gamma = 0$. What is the required common mode input for which $R_{SS}$ sustains 0.5 V?

(5+3+2)

2A. Give the circuit of double cascode current sink. Using small signal ac model, derive the expression for output resistance. What is the minimum output voltage across the current sink?

2B. Explain the channel length modulation. Derive the expression for channel length modulation parameter ($\lambda$).

2C. Calculate the small signal voltage gain of the circuit shown in FIG. 2C.

(5+3+2)

3A. Give the schematic circuit of a PMOS based folded cascode amplifier. Derive the exact expression for small-signal voltage gain and output resistance. Also give the approximate expression for voltage gain.

3B. [i] Explain how the nonlinearity in CS stage is minimized using source degeneration.

[ii] Obtain the expression for small-signal voltage gain for NMOS CG amplifier stage with diode connected PMOS active load for following cases: (i) $\lambda \neq 0, \gamma \neq 0$ (ii) $\lambda = 0 , \gamma = 0$

3C. Calculate the gain of the circuit in FIG. 3C at very low and very high frequencies neglecting all other parasitic capacitances. Assume $\lambda = \gamma = 0$.

(5+3+2)

4A. Discuss the frequency response of common source amplifier by considering high-frequency small signal analysis.

4B. With a schematic circuit explain the working of an unbalanced CMOS OTA. Give the expression for dominant and non-dominant pole frequency. Bring out the differences between unbalanced and balanced OTA.

4C. Discuss the structure of poly-poly capacitor.

(5+3+2)

5A. [a] State and prove Miller's theorem

[b] Explain the following analog layout techniques [i] interdigitization [ii] symmetry

5B. Discuss the function of RF Mixer. Discuss the differential amplifier based mixer topology.

5C. Why standard Digital CMOS is preferred for RF IC design?

(5+3+2)

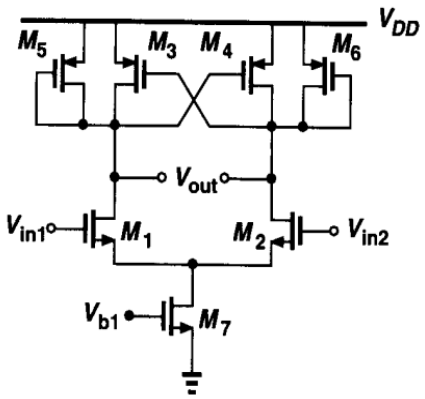


**FIG. 1 B**

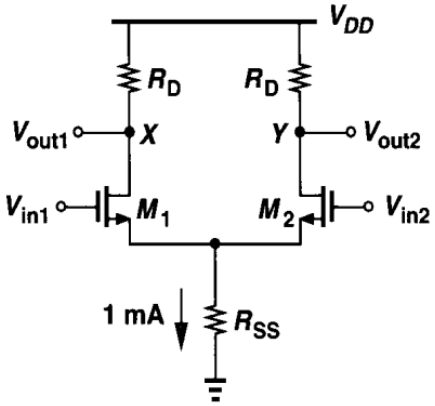


**FIG. 1C**

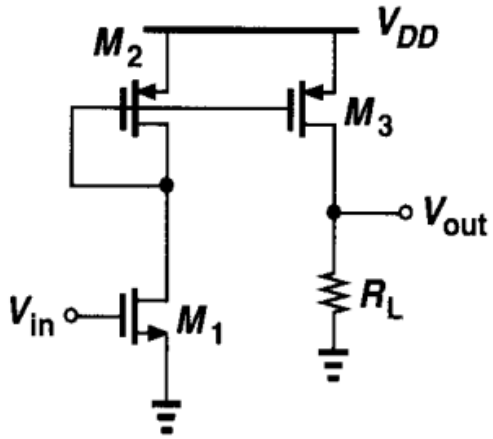


**FIG. 2C**

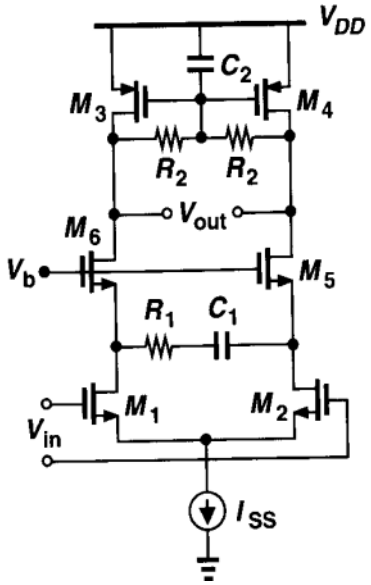


**FIG. 3C**