Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

FIRST SEMESTER M.TECH (DEAC & Micro Electronics)
END SEMESTER EXAMINATION - NOV/ DEC 2016
SUBJECT: ANALOG AND RF VLSI DESIGN (ECE - 5102)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. [a] Derive the expression for small-signal voltage gain and output resistance of a NMOS CS amplifier with diode connected NMOS active load.

[b] Explain how the differential operation can reduce following: [i] effect of supply noise [ii] Effect of coupled noise from digital clock signal

1B. Find the expression for resistance **Z** for the circuits shown in **FIG. 1B**.

1C. In a NMOS CD amplifier with a current sink load, all transistors have W/L=100 µm/ 2 µm. Given that I_{ref} =100 µA, η = 0.1, K_n = 75 µA/V^2, K_p = 30 µA/V^2, $r_{ds\text{-}n}$ = 128 kΩ, $r_{ds\text{-}p}$ = 192 kΩ. Find A_v, R_{out}.

(5+3+2)

2A. [a] Define and explain the significance of following parameters with respect to MOS device: [i] γ [ii] η [iii] L_{drawn} [iv] L_{eff}

[b] Define the following parameters. Give their units

[i] LAMBDA [ii] Early voltage

2B. (i) What do you understand by "cascode" topology ? Explain the telescopic PMOS double cascode amplifier with NMOS cascode load. State the merits of the circuit.

(ii)Explain the concept of following: [i] simple folded cascode amplifier [ii] folded cascode amplifier with biasing.

2C. Derive an expression for sensitivity of output current I_o with respect to V_{DD} in a cascode current sink circuit. Explain the significance of this sensitivity expression?

(5+3+2)

3A. [a] Consider the schematic circuit of a NMOS differential amplifier using M_1-M_2 differential pair with a M_3-M_4 current source load. Given that $(W/L)_{1,2}$ = 50/10, $(W/L)_{3,4}$ = 10/10, K_n = 40 µA/V^2, μ_n = 2.5 μ_p , I_b = 10 µA, $\lambda_{n,p} = 0.05\ V^{-1}$. Find the following: [i] Circuit transconductance G_m [ii] Output resistance R_o [iii] Differential voltage gain

[b] Define the following with respect to MOS devices: (i) transconductance (ii) ouput conductance (iii) intrinsic gain. Mention their units.

3B. Calculate the gain of the circuit in **FIG. 3A** at very low and very high frequencies neglecting all other parasitic capacitances. Assume $\lambda = \gamma = 0$.

3C. Explain the effect of following as applied to current mirrors: [i] lateral diffusion [ii] oxide encroachment.

(5+3+2)

4A. [i] Explain the working of CMOS Double-balanced Mixer

[ii] State why long channel devices are used in analog design?

4B. [i] Explain the basic PLL block diagram with necessary analog building blocks.

[ii] State the principle used in the design of RF Mixers.

4C. Compare OTA and op-amp with respect to following: [i] area [ii] input and output resistance [iii] gain [iv] bandwidth

(5+3+2)

5A. Consider a NMOS CG amplifier with a passive resistive load R_D. Derive the expression for following: (i) small-signal voltage gain (ii) input impedance (iii) output impedance considering with and without channel length effect. Give your comments

5B. [a] Give the circuit of two-stage Operational Transconductance Amplifier (OTA) circuit.

[b] Explain the following analog layout techniques [i] common centroid geometry [ii] dummy strip

5C. Explain the use of following analog blocks: [i] VCO [ii] RF synthesizers

(5+3+2)

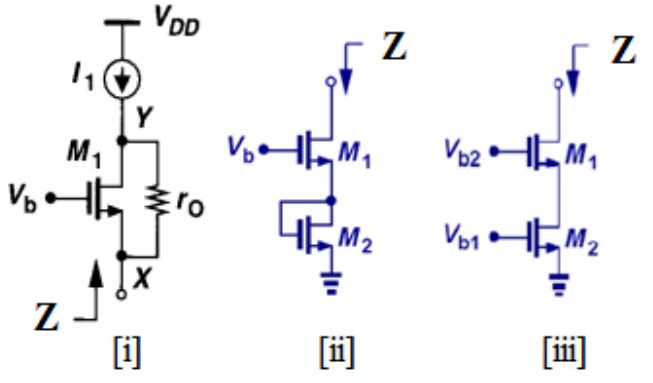

FIG. 1B

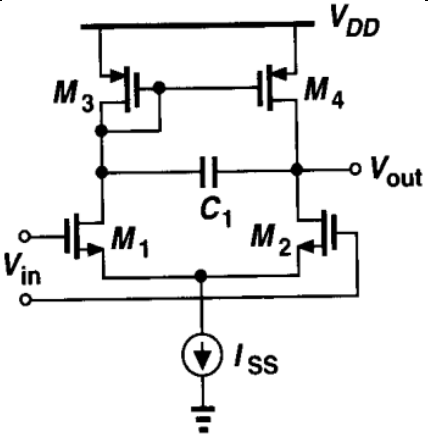

FIG. 3A