Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

FIRST SEMESTER M.TECH (DEAC & ME) DEGREE END SEMESTER EXAMINATION - NOV/DEC 2016

SUBJECT: PROCESSOR ARCHITECTURE & APPLICATIONS (ECE – 5103)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. A superscalar pipelined machine, capable of fetching and decoding two instructions at a time, having three functional units (F1 & F2 are 2 integer + F3 is a 1 floating point). Each instruction takes one cycle to execute. Two instances of write back stages.

Given: Ten instruction code segment (I1 to I10)

- I3 and I4 conflict for functional unit F3
- I5 depend on value produced by I4
- I5 and I6 conflict for functional unit F2
- I7 and I8 also conflict for functional unit F2
- I9 and I10 conflict for functional unit F1

Implement the above code using **two policies** which take minimum number of clock cycles.

1B. What is the significance of register renaming technique in instruction level parallelism? Explain.

1C. Discuss different pipeline hazards with examples.

(4+4+2)

2A. Describe architectural overview and on chip memory of TMS320C62x DSP Processor.

2B. Discuss architecture and instructions of a processor, which uses registers for all vector operations except for load and store.

2C. Explain Polling based I/O strategy with algorithm / program used for implementation.

(4+4+2)

3A. What is MMU? Explain the following, with necessary diagrams.

i) Different types of page tables.
ii) Different page table entries
iii) Two step page table walk with L2 coarse page table

3B. What are the different parallel architectures followed in multiprocessors based on instructions and data stream? Also explain multiprocessor structures based on memory organizations and their interconnect strategy.

3C. In a coherent centralized memory based multiprocessor scheme, four processors W, X, Y, Z are connected to a memory. Initial content of memory location M is FFH. CPU X reads the content of memory location M and then writes 00 to M. With the help of different protocols, narrate the bus activities and updating of contents in caches of different processors.

(4+4+2)

4A. Write a programming model/architecture of MSP 430 microcontroller and discuss it's application.

4B. Discuss different factors effecting cache optimization and solutions to overcome them.

4C. 8 KB I & D cache.
Instruction miss rate = 0.64%. Data miss rate = 6.47%.
Hit time = 1. Miss time = 50.
90 % accesses are from instructions.

16KB unified cache.
Aggregate miss rate = 1.99%.
Hit time = 1. Miss rate = 50.
90 % accesses are from instructions.
Which one is better?

(4+4+2)

5A.
1. Instruction sequence 1
   lw $1, 50 ($7)
   add $7, $2, $2
   sw $7, 50($1)
2. Instruction sequence 2
   lw $3, 15 ($3)
   sw $3, 15($3)
   add $3, $3, $8

For the above code sequence 1 and 2, only ALU – ALU forwarding allowed (No forwarding from MEM to EX stage). If no ALU – ALU forwarding possible, then add 'NOP' instructions to eliminate hazards. Show schematic diagram. Determine total number of clock cycles required to implement the code sequence.

5B. With abstract diagrams, analyse execution of instructions using multicycle implementation scheme. Discuss its advantages.

5C. Discuss overflow / underflow solutions associated with MAC unit in a DSP Processor.

(4+4+2)