Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

V SEMESTER B.TECH. (COMPUTER SCIENCE AND ENGINEERING)

END SEMESTER EXAMINATIONS, NOV/DEC 2016

SUBJECT: **COMPUTER ARCHITECTURE** [CSE 3101]

REVISED CREDIT SYSTEM
(27/12/2016)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitable assumed.

1A. Explain the sequence of events that happen during an instruction cycle when fetch and interrupt occurs with a neat diagram. **3M**

1B. Consider the execution of program of 1,50,000 instructions by a linear pipeline processor with a clock rate of 1000MHz. Assume that the instruction pipeline has five stages and that one instruction is issued per clock cycle. The penalties due to branch instructions and out of sequence executions are ignored.
a) Calculate the speedup factor using this pipeline to execute the program as compared with the use of an equivalent non-pipelined processor with an equal amount of flow through delay.
b) What are the efficiency and throughput of this pipeline processor? **3M**

1C. Give an example of the parallel architecture which exploits spatial parallelism and temporal parallelism. Explain the same with a neat diagram. **4M**

2A. Explain Feng's classification of computers with its various processing methods and necessary equations. **3M**

2B. List the dependences in the respective table given below by writing in the instruction numbers involved with the dependence.
I0: A = B + C;
I1: C = A - B;
I2: D = A + C;
I3: A = B * C * D;
I4: C = F / D;
I5: F = A ^ G;
I6: G = F + D; **3M**

RAW Dependence		WAR Dependence		WAW Dependence	
From Instruction	To Instruction	From Instruction	To Instruction	From Instruction	To Instruction

2C. For the collision vector C= 101010
a) Find all forbidden latencies
b) Draw the state transition diagram
c) Find all the Simple cycles and Greedy cycles.
d) Determine MAL.
e) If pipeline clock period is 20ns. Find the maximum throughput of the pipeline.

4M

3A. Find the sum of the numbers given below using an array of 5 processing elements. Write the algorithm and masking scheme for the same.

PE1	PE2	PE3	PE4	PE5
1	24	5	7	18

3M

3B. With a neat schematic diagram, explain Burrough's Scientific Processor. Design a Barrel Shifter network for 16 processors.

3M

3C. For N=8 processing elements, explain the working and the permutation cycle of perfect shuffle and exchange routing functions with a neat diagram. Also draw a single stage recirculating shuffle-exchange network.

4M

4A. List and explain the features of multistage networks.

3M

4B. Explain the following :
a) Software cache coherent schemes
b) Write Miss

3M

4C. Briefly describe the different approaches to multithreading

4M

5A. With a neat diagram explain the general structure of Intel Core Duo.

3M

5B. At a top level, what are the main design variables in a multicore organization? List any three advantages of a shared L2 cache among cores compared to separate dedicated L2 caches for each core.

3M

5C. Explain briefly the different clustering methods.

4M