Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

FIFTH SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION
NOV/DEC 2016
SUBJECT: COMPUTER ORGANIZATION AND ARCHITECTURE (ECE - 3106)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Draw the typical stack based machine. Using a minimum number of zero address instructions, write a program for the given expressions:
i) Z= (A* B + C)*D+ E/F
ii) Z= A*(B+C+D+E)- F
Show the stack operations.

1B. Given the symbol probabilities, $g_0 = 0.2$, $g_1 = 0.3$, $g_2 = 0.1$ and $g_3 = 0.4$. Perform encoding for the symbols using Huffman's encoding. Calculate the redundancy of Block code and Huffman code for these symbols and compare.

1C. Fill the following table for the given adder design. Assume, gate delay=clock period = 5 µ sec, CSA add time is half of the CPA time. Consider CSA add time is 20 µ sec .Full adder time is 10µsec

Sl.No	Adder type	Total delay
1	16 bit Ripple carry adder	
2	16 bit Carry look ahead adder	
3	8 operand Carry save adder	
4	16 bit, 4 operand Series parallel adder	

(5+3+2)

2A. Perform the following: i) Divide 43 by 7 ii) Multiply -43 with +32 using Modified Booth's algorithm. Iii) Convert the following decimal number to 32-bit IEEE floating point representation:
– 0.00125

2B. Construct CSA adder circuit using FA blocks for adding four, 4-bit signed numbers as ***p, q, r*** and ***s***. Find the delay of this circuit.

2C. Design and implement a combinational circuit using logic function blocks that will work as follows: Assume A and B are 4 bit data:

S1	S0	Function
0	0	A *plus* B
0	1	*Shift left* (A)
1	0	A *minus* B
1	1	*Shift left* (A) + 1

(5+3+2)

3A. Design a hardwired Controller for the following algorithm:
Declare registers A[8],B[8],C[8];

START: A← 0, B←00001010;

LOOP:A←A+B;

B←B-1;

If B< > 0 then go to LOOP

C←A;

HALT: Go to HALT

3B. Explain the organization of General-purpose Micro-programmed Control with a neat diagram.

3C. Explain the PLA Implementation of Sequence Controller Design for Booth's Multiplier.

(5+3+2)

4A. Differentiate between: i) Standard IO and Memory mapped IO. ii)Internal and external interrupts iii)Polled interrupts and Daisy chain interrupts iv) Conditional and unconditional programmed IO v) Cycle stealing and interleaved DMA

4B. A computer system needs an 8MB RAM. Assuming 64K×4 RAM chips are available, show how to build required RAM. Draw a neat logic diagram of your implementation showing the address, data, control signals and chip select logic.

4C. A set associative cache has a total of 64 blocks divided in to sets of 4 blocks each. Main memory has 1024 blocks with 16 words per block. How many bits are needed in each of the tag, set and word fields of the main memory address? (5+3+2)

5A. Explain instruction pipeline and pipeline hazards. Justify how pipeline improves the performance of a processor.

5B. Draw the typical array processor organization and explain.

5C. Write the differences between paging and segmentation. (5+3+2)