Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
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FIFTH SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION
NOV/DEC 2016
SUBJECT: COMPUTER ORGANIZATION AND ARCHITECTURE (ECE - 3106)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. For the expression G = (A+B*C)/(D-E*F), write the program for register based, accumulator based and stack based machine. Fill the following table, assuming the size of the op code field is 8 bits, A, B, C, D, E, F, G refer to either 20 bit memory address or 3 bit register address.

	Register based machine		Accumulator based	Stack based
No of instructions				
Program size in bits				
No of distinct registers used				

1B. A computer follows 16-bit instruction length and address field of 4-bit. There are 34 two address instructions and 100 one address instructions are encoded using expanding opcode technique. Find the number of zero address instructions that can be supported.

1C. Give the example instructions for the following addressing modes: immediate, register, direct, register indirect, indexed, relative, base register, auto-indexed

(5+3+2)

2A. i) For the function table given below, design a 4 bit general register of Booth's multiplier:

S1	S0	Function
0	0	Clear
0	1	Decrement
1	0	Arithmetic. Right shift
1	1	Load external data

ii) Perform multiplication on - 48 x 56 using Booth's algorithm. Show all the iterations. Verify your answer using bit pair recoding method.

2B. Write a Wallace tree structure for adding seven single bit numbers; named as W7. Using W7 blocks, write a structure for adding eight, 2 bit numbers.

2C. Design a combinational circuit that will satisfy the following specifications: X (input) and Y (output) are 4 bit data.

S1	S0	Y
0	0	X
0	1	X
1	0	0
1	1	0

(5+3+2)

3A. Design and implement an 8-bit ripple carry adder using 4-bit adder blocks. Assuming two and three gate delay for getting carry and sum respectively for every FA within 4-bit adder, find the delay involved in the generation of the final sum of the above 8-bit adder. Draw 4 bit CLA. Using 4-bit CLA blocks, construct an 8-bit adder circuit and compare the delay.

3B. Design a Micro-programmed Control unit for the following algorithm:
Declare registers A[8],B[8],C[3], Inbus [8], Outbus[8];

START: A← 0, B←Inbus, L←4;

LOOP:A←A+B,C←C-1;

If C< > 0 then go to LOOP

Outbus←A;

HALT: Go to HALT

3C. Implement the hardware for the following control statements, where X,Y, A, B, D are 4 bit numbers.

i) If X=0 and Y[0]=1, then A← B else A ← D ii) C_o: A ← B Where C_o = (A>B) AND D[0][1]

(5+3+2)

4A. A typical computer system has a 64MB of main memory and a 32kB of fully associative cache memory. The cache line size is 8 bytes. The access time of the main memory is 10 times that of the cache memory.

i) What is the size of the tag field?
ii) If direct mapping scheme is used instead, what would be the size of the tag field?
iii) If four-way set associative mapping is used, show the format of memory address.
iv) Determine the access efficiency, assuming a cache hit ratio of 0.9.
v) If the cache access time is 100 ns, what hit ratio would be required to achieve an average access time equal to 250 ns.

4B. What are the different ways to handle multiple interrupts from several I/O devices? Explain each technique with neat sketches and example.

4C. Explain paging and segmentation systems.

(5+3+2)

5A. Explain the following: i) Pipeline hazards ii) Array processor organization iii) VLIW architecture

5B. Draw various bus organization structures and explain how the speed of instruction execution improves.

5C. In a 5 stage pipeline organization, if 25% of the instructions are branch instructions, compute the average number of instructions computed per instruction cycle.

(5+3+2)