Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

FIFTH SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION - NOV/DEC 2016
SUBJECT: MICROCONTROLLER (ECE - 3102)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Describe all the addressing modes supported by 8051 with examples.
1B. Describe the Architecture of typical Advanced Microcontroller Bus in ARM core.
1C. Draw the CPSR format of ARM & explain each bit.

(5+3+2)

2A. Write an assembly language program in 8051 for arranging ten 8-bit numbers which are stored in the external RAM starting from 8000H in ascending order. Assume that array length is 10 bytes.
2B. With neat diagram, explain the clock generation for the LPC1768.
2C. Describe the possible methods to start and stop the timers operation in 8051 microcontroller with relevant diagram.

(5+3+2)

3A. Write an ALP for LPC1768 to generate 8-bit ring counter through GPIOs P0_0 to P0_7.
3B. Write a program to transmit the message "HELLO" serially at 4800 baud rate, 8-bit data and 1 stop bit continuously. Assume that crystal frequency of 8051 microcontroller is 11.0592 MHz.
3C. Explain the following Assembler directives of ARM with an example for each
i). RN ii) EQU iii) ALIGN iv) DCW

(5+3+2)

4A. A DC motor (to P1.0) and two switches (SW0 and SW1 to P2.0 and P2.1 respectively) are interfaced to 8051. Write an assembly language program to monitor the status of the switch and perform the following:

SW1	SW0	Speed of the motor
0	0	DC motor rotates slowly (25% duty cycle)
0	1	DC motor rotates moderately (50% duty cycle)
1	0	DC motor rotates fast (75% duty cycle)
1	1	DC motor rotates very fast (100% duty cycle)

4B. If more than one interrupts are generated simultaneously, explain how 8051 handles such interrupts. Is it possible to alter the default priority order in 8051? If yes explain how this can be achieved.
4C. Describe the functions of each bit in the following SFRs with bit diagram: TCON, SCON

(5+3+2)

5A. Write and explain the 32-bit binary encoded format of the ARM instruction:
ADDS R1, R2, R3, LSL R4.

5B. Explain ARM data path activity of the instruction LDR R1, [R2, 0x24]!

5C. Write differences between ARM & THUMB states of ARM processor.

(5+3+2)