Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

FIFTH SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION NOV/DEC 2016
SUBJECT: VLSI PT (ECE - 323)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ANY FIVE** full questions.
- Missing data may be suitably assumed.

1A. Explain the Czochralski Technique of wafer fabrication.

1B. How (i) penumbral blur (ii) lateral magnification error in X-ray lithography will degrade the quality of resist?

(6+4)

2A. Determine the time needed to grow 0.35 μm of oxide on a bare silicon wafer (i.e. no initial oxide) if the oxidation temperature is 1000°C. The wafer has (100) orientation. Find the times for both wet and dry oxidations. Given,

Ambient	B	B/A
Dry O_2	$C_1 = 7.72 \times 10^2\ \mu^2\ hr^{-1}$ $E_1 = 1.23$ eV	$C_2 = 6.23 \times 10^6\ \mu\ hr^{-1}$ $E_2 = 2.0$ eV
Wet O_2	$C_1 = 2.14 \times 10^2\ \mu^2\ hr^{-1}$ $E_1 = 0.71$ eV	$C_2 = 8.95 \times 10^7\ \mu\ hr^{-1}$ $E_2 = 2.05$ eV
H_2O	$C_1 = 3.86 \times 10^2\ \mu^2\ hr^{-1}$ $E_1 = 0.78$ eV	$C_2 = 1.63 \times 10^8\ \mu\ hr^{-1}$ $E_2 = 2.05$ eV

2B. (i) Consider the conventional MASK as shown in Figure 2B. What is the problem encountered in conventional mask design during optical lithography and how it is rectified by Phase shifting Mask design.

(ii) Draw the Amplitude at MASK, at wafer and intensity at wafer for both the cases.

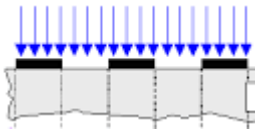

Figure 2B.

(6+4)

3A. (i) Do thinner resists layers improve or degrade lithography resolution? Explain.

(ii) How does optical proximity correction improve the resolution of lithography? How do Contrast Enhancement Layers improve resolution?

(iii) Discuss the advantages and disadvantages of electron-beam lithography.

3B. (i) Figure 3B shows the etch profile of silicon using hot KOH as etchant. 1) What is the Miller index for plane A ? 2) What is the Miller index for plane B ? 3) What is the best etching mask material for this etching process?

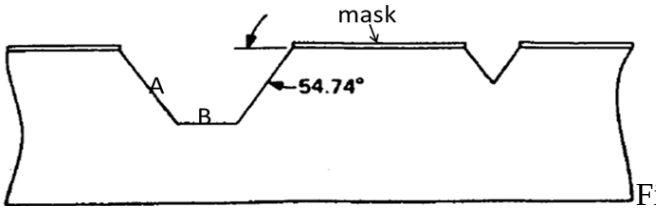

Figure 3B.

(ii) For CVD deposition of silicon using SiH4 gas, what is the chemical reaction? Why the deposition rate is faster using N2 carrier gas than using H2 carrier gas?

(6+4)

4A. Explain the process of reactive ion etching.

4B. Explain the fabrication of MOS capacitor with neat diagram.

(6+4)

5A. (i) You wish to dope a single crystal of silicon (Si) with boron (B). The specification reads 5×10^{16} boron atoms/cm^3 at a depth of 25 μm from the surface of the silicon.

What must be the effective concentration of boron in units of atoms/cm^3 if you are to meet this specification within a time of 90 minutes?

Assume that initially the concentration of boron in the silicon crystal is zero. The diffusion coefficient of boron in silicon has a value of 7.23×10^{-9} cm^2 /s at the processing temperature.

(ii)A boron diffusion into a 1-ohm-cm n-type wafer results in a Gaussian profile with a surface concentration of 5×10^{18} cm^{-3} and a junction depth of 4μm. Given, $N_B = 4.5 \times 10^{15} cm^{-3}$, D_0=10.5 cm^2/s, Ea=3.69 eV.

5B. (i) Explain emitter-push effect with neat diagram.

(ii) Why ion implantation (rather than gas phase diffusion) is used for microprocessor manufacturing?

(6+4)

6A. 200 keV phosphorus (Rp=0.254μm, ΔRp=0.0775μm) is implanted into a p-Si (boron doping $C_B=10^{16}$ cm^{-3}) with a dose of 10^{13} cm^{-2}. i) Find the peak concentration (cm^{-3}). ii) Find the p-n junction depth (there might be two junctions, if so, find both). iii) Find the sheet resistance. Assume electron mobility of 800 cm^2/V·sec.

6B. (i) What is the single most important advantage of LPCVD over APCVD?

(ii) For CVD deposition of silicon using SiH_4 gas, what is the chemical reaction?

(6+4)