Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

FIFTH SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION - NOV/ DEC 2016
SUBJECT: VLSI DESIGN (ECE - 305)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **any five full** questions.
- Missing data may be suitably assumed.

1A. Explain the transfer characteristic of the CMOS inverter showing different regions. For CMOS inverter, derive the expression for V_{inv}.

1B. Compare BJT and MOSFET with respect to following parameters:
(i) Transconductance value (ii) Input impedance (iii) Noise (iv) Current handling capability

1C. Discuss the influence of β_n/β_p on inverter DC transfer characteristic.

(5+3+2)

2A. Explain the steps involved in the twin-tub fabrication process. What is the use of epitaxial layer?

2B. Calculate the effective capacitance for the multi-layer structure given in **FIG. 2B** for 5 µm process. Refer the **Table I** for area capacitance calculation.

2C. Draw stick notation for [i] Depletion type pull-up NMOS inverter [ii] Single phase Pre-charge Evaluate Dynamic CMOS two-input NOR gate

(5+3+2)

3A. Derive Z_{pu} / Z_{pd} ratio for Pseudo NMOS inverter driven from a similar inverter.

3B. Explain the working of 6T SRAM cell.

3C. Find the region of operation for NMOS based circuits given in **FIG. 3C**. Assume $V_T = 0.4V$

(5+3+2)

4A. [i] The NMOS transistors in the circuit of **FIG. 4A** have $V_{thn} = 1$ V, $\mu_n C_{ox} = 120\ \mu A/V^2$ and $L_1 = L_2 = L_3 = 1$ µm. Find the required values of gate width for each of Q_1, Q_2 and Q_3 to obtain the voltage and current values indicated.
[ii] State the advantages of transmission gate over NMOS/PMOS pass transistors.

4B. Justify as why the NOR gate is preferred over NAND gate for the implementation of NMOS PLA. Explain with an example.

4C. Give the CMOS implementation and stick notation for the function $Z = (A\,B + C)'$.

(5+3+2)

5A. Give the implementation of NMOS based R/2 stage shift register cell and explain the working principle. Give the stick notation and layout of the NMOS based R/2 stage shift register cell.

5B. With a truth table, give the NMOS implementation of NOR based SR latch

5C. Give the NMOS implementation of following functions: $F = \overline{AB\bar{C} + D}$ and $Y = A \odot B$.

(5+3+2)

6A Explain structured implementation of N-bit bus arbitration logic. Give the stick notation. Discuss the suitability of implementation using NMOS/ CMOS technology.

6B Give the implementation of two-input NOR gate using BiCMOS.

6C Give an account of different trends in VLSI technology.

(5+3+2)

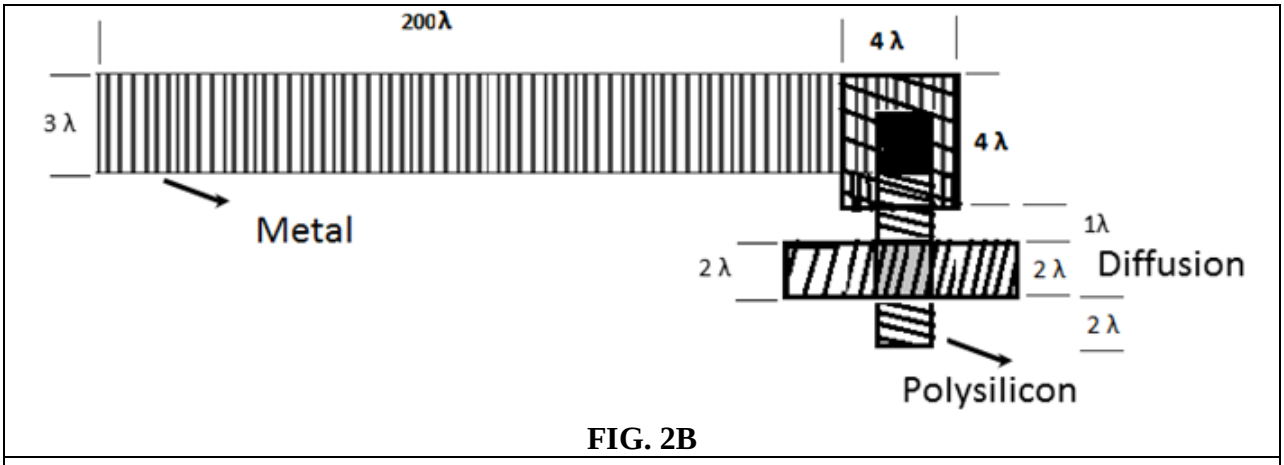

FIG. 2B

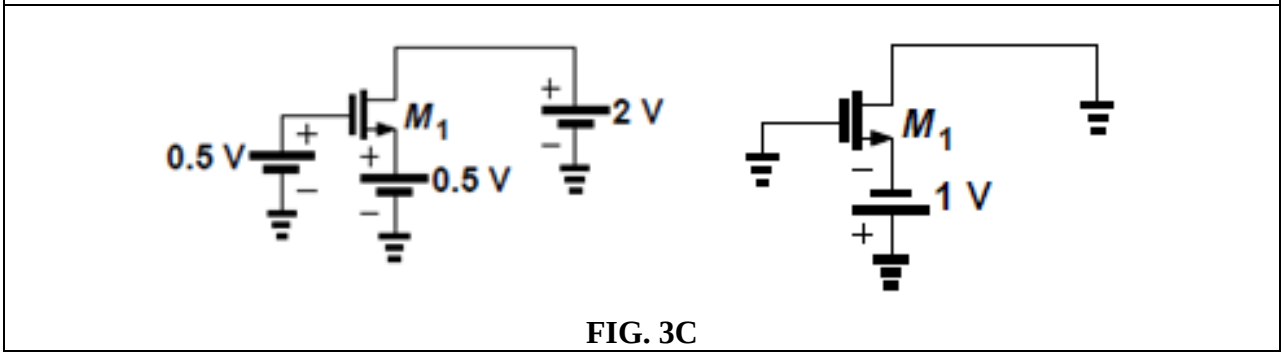

FIG. 3C

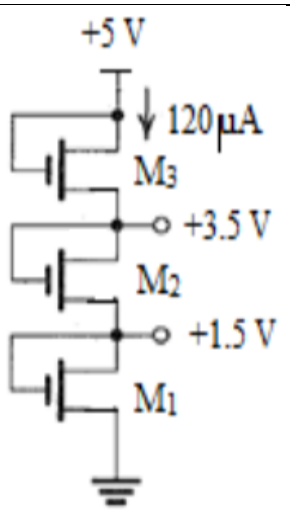

FIG. 4A

Table I Typical values of area capacitance for 5 μm technology

Capacitance	*Value in pF* $\times 10^{-4}/\mu m^2$ *(Relative values in brackets)*	
Gate to channel	4	(1.0)
Diffusion (active)	1	(0.25)
Polysilicon* to substrate	0.4	(0.1)
Metal 1 to substrate	0.3	(0.075)
Metal 2 to substrate	0.2	(0.05)
Metal 2 to metal 1	0.4	(0.1)
Metal 2 to polysilicon	0.3	(0.075)