Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

FIFTH SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION - NOV/ DEC 2016

SUBJECT: VLSI DESIGN (ECE - 305)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **any five full** questions.
- Missing data may be suitably assumed.

1A. With neat figures, explain the steps involved in fabrication process of Enhancement type NMOS transistor

1B. Explain the transfer characteristic of the CMOS inverter showing different regions. Discuss how the transfer characteristic is affected by aspect ratio of n-type and p-type devices.

1C. Bring out differences between Constant E field and Constant V scaling.

(5+3+2)

2A. Derive Z_{pu} / Z_{pd} ratio for pseudo NMOS inverter driven from a similar inverter.

2B. For a CMOS Inverter having $L_n = L_p = W_n = 2\ \mu m$, $W_p = 5\ \mu m$. Compute the following:

(i) rise time t_r (ii) fall-time t_f (iii) total delay T_d through a pair of inverters.

Given the typical sheet resistance and standard capacitance values for 2 µm process:

[i] NMOS channel resistance = 20 kΩ/ square [ii] PMOS channel resistance = 45 kΩ / square

[iii] Gate-to-channel capacitance = 8 pF x 10^{-4}/ μm^2

2C. Find the region of operation for the circuit given in **FIG. Q 2C** (i) and (ii). Threshold voltage V_{TH} = 0.4 V.

(5+3+2)

3A. Two CMOS inverters are cascaded to drive a capacitive load $C_L = 40 C_g$ as shown in **FIG. Q 3A**. Find the Z_{pu} and Z_{pd} of each inverter. Calculate the pair delays in terms of τ for the inverter geometry indicated.

3B. Give the schematic and equivalent stick notation of 1-bit CMOS shift register cell.

3C. Define a two-phase non-overlapped clock with waveforms. Give a circuit to generate the same.

(5+3+2)

4A. Compute and compare the minimum size NMOS and CMOS inveter pair delay.

4B. (i) State Moore's Law and explain its significance in VLSI.

(ii) Give the stick notation of 2 input NMOS NAND gate.

4C. Explain the following terms.

(i) Transconductance (ii) Channel length effect

(5+3+2)

5A. Give the circuit implementation of following multiple output function using NMOS based PLA. Give the stick notation. $Z_1 = ABC + \overline{A}\overline{B}C$; $Z_2 = ABC$; $Z_3 = A + \overline{B}C$

5B. Draw the NMOS Layout of 2-to-1 data selector.

5C. Give two-stage NMOS implementation of XOR gate without needing complemented input variables.

(5+3+2)

6A What is a cross-bar switch? Bring out the differences between barrel shifter and cross-bar switch. Give the circuit implementation and the stick notation of 4X4 barrel shifter.

6B Give the stick notation for circuit implementation of 4:1 data selector using NMOS switches

6C Show that the delay associated with the N-input NMOS NAND gate is given by $\tau_{nand} = N.\tau_{inv}$ where τ_{inv} is the corresponding NMOS inverter delay.

(5+3+2)

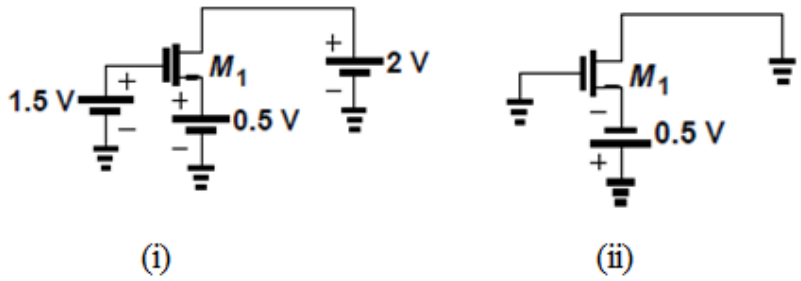

FIG. Q 2C

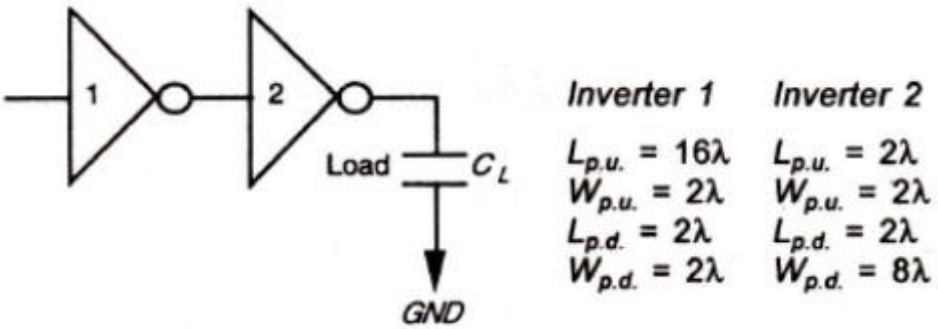

FIG. Q 3A