Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

FIFTH SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION - NOV/ DEC 2016
SUBJECT: VLSI DESIGN (ECE - 3104)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Explain the fabrication process of CMOS inverter using SOI technique with all necessary steps and diagrams. State any two advantages of SOI process over traditional CMOS.

1B. Explain the transfer characteristic of the CMOS inverter showing different regions. Discuss how the transfer characteristic is affected by aspect ratio of n-type and p-type devices.

1C. The NMOS transistors in the circuit of **FIG. 1C** have V_{thn} = 1 V, $\mu_n C_{ox}$ = 120 μA/V^2 and $L_1 = L_2 = L_3$ = 1 μm. Find the required values of gate width for each of Q_1, Q_2 and Q_3 to obtain the voltage and current values indicated.

(5+3+2)

2A. [i] What is a capacitive cross talk? Explain the effects of cross talk noise due to floating victim and driven victim.
[ii] Explain the impact of inductance on supply voltages.

2B. Refer the multilayer structure given in **FIG. 2B**. Given that λ = 2.5 μm. Refer the **Table I** for area capacitance calculation.
(i) A 3λ wide metal path crosses a 2λ wide polysilicon path at right angles. The layers are separated by a 0.5 μm thick layer of silicon dioxide. Find the capacitances associated with metal layer.
(ii) The polysilicon layer in turn crosses a 4λ wide diffusion region at right angles to form a transistor. Find the capacitance associated with poly layer.

2C. Draw stick notation for [i] Pseudo NMOS inverter [ii] Single phase Pre-charge Evaluate dynamic CMOS two-input NOR gate

(5+3+2)

3A. Implement the following functions and mention appropriate L/W ratio of each transistor
(i) $F = (a + b.c)'$ using pseudo NMOS with pull-up ratio is 1/3.
(ii) $F = (a_1 + a_2)(a_3 + a_4) \ldots \ldots (a_{n-1} + a_n)$ up to n stages using cascaded Domino CMOS logic.
(iii) $F = a + (b.c)'$ using clocked CMOS logic.
(iv) An N-input NOR gate using dynamic CMOS logic for $\beta_n \neq \beta_p$.
(v) The function corresponding to the set of input and output waveforms given in **FIG. 3A** using NMOS switch logic.

3B. Explain the WR and RD operation of 6T sRAM cell.

3C. Define a two-phase non-overlapped clock with waveforms. Give a circuit to generate the same.

(5+3+2)

4A. Implement a 4-bit ALU using full adder as standard cell and implement the following :

(i) A or B (ii) A exnor B

4B. Implement following words: word1: 0110, word2: 0010, word3: 1101, word4: 0101 using pre-charge NMOS ROM. Draw the layout of one cell.

4C. Identify the circuit given in **FIG. 4C** and explain the working principle. Note that C_X and C_Y are the parasitic capacitances and $\boldsymbol{C_L}$ is the load capacitance. If $C_X = C_Y = 0.3\,C_L$. Find the output voltage value evaluated for a case of A B C = 1 1 0.

(5+3+2)

5A. Give the implementation of NMOS based R/2 stage shift register cell and explain the working principle. Give the stick notation and layout of the NMOS based R/2 stage shift register cell.

5B. [i] Draw the circuit arrangement of 4x4 cross bar switch. Draw the layout of standard cell.
[ii] Define regularity. What is the regularity factor of 8 x 8 bit barrel shifter?

5C. Identify the MOS structures given in FIG. 5C and give your comments.

(5+3+2)

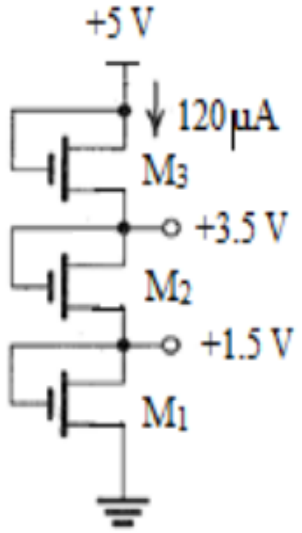

FIG. 1C

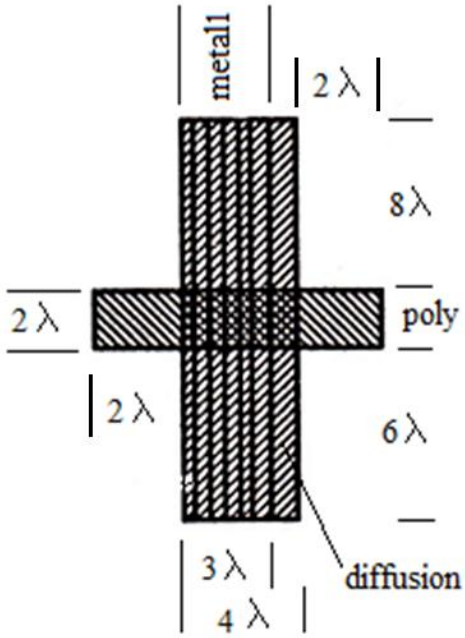

FIG. 2B

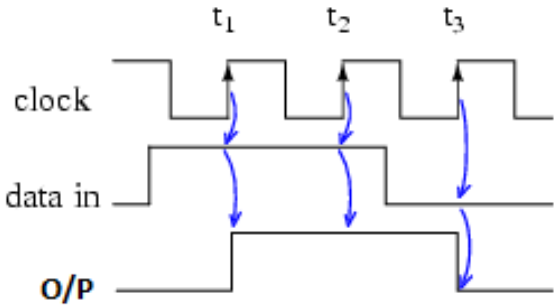

FIG. 3A

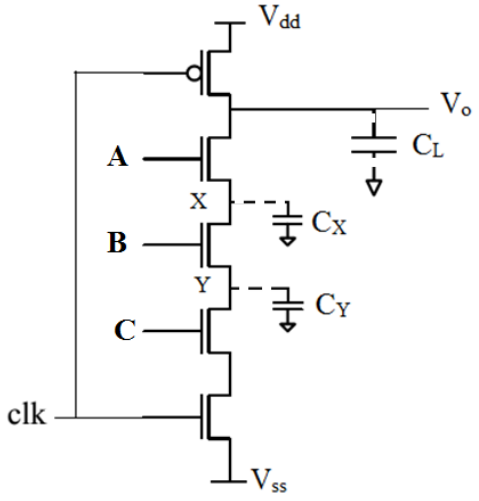

FIG. 4C

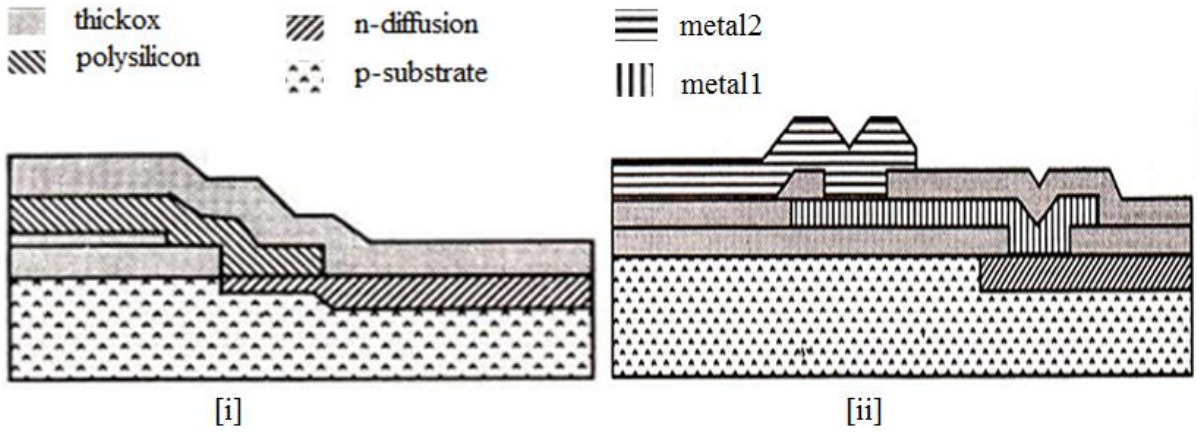

FIG. 5C

Table I Typical values of area capacitance for 5 µm technology

Capacitance	*Value in pF × $10^{-4}/\mu m^2$ (Relative values in brackets)*	
Gate to channel	4	(1.0)
Diffusion (active)	1	(0.25)
Polysilicon* to substrate	0.4	(0.1)
Metal 1 to substrate	0.3	(0.075)
Metal 2 to substrate	0.2	(0.05)
Metal 2 to metal 1	0.4	(0.1)
Metal 2 to polysilicon	0.3	(0.075)