Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

FIFTH SEMESTER B.TECH (INSTRUMENTATION & CONTROL ENGG.)

END SEMESTER EXAMINATIONS, DEC 2016/JAN 2017

SUBJECT: DIGITAL SYSTEM DESIGN [ICE 311]

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

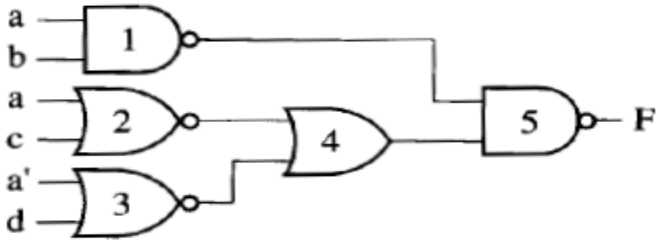
- Answer **ANY FIVE FULL** questions.
- Missing data may be suitably assumed.

1A. Find the minimum sum of products using Karnaugh map for the following function: **3**

$$F(A,B,C,D) = \sum m(0,2,3,5,6,7,8,10,11) + \sum d(14,15)$$

Note:'d' represents don't care in the function.

1B. Write a VHDL description of the folllowing combinational network using concurrent statements. **3**



1C. Illustrate the working of different types of tristate buffers with diagrams. **4**

2A. Explain how variables, signals and constants are declared in VHDL with examples. **3**

2B. Draw a complete Y-chart showing different levels and domains of abstraction. **4**

2C. Explain the Mealy and Moore sequential networks listing their differences. **3**

3A. Write VHDL code for a full adder using logic equations. **3**

3B. Write a sequential VHDL code for D flip-flop. **4**

3C. Explain functions in VHDL with sample code. **3**

4A. Write a structural VHDL code for a full subtracter assuming that full subtracter has been defined as a component. **4**

4B. How are arrays declared in VHDL? Write a VHDL code for finding the greatest value in an array. **3**

4C. Write a test bench to verify the working of T flip-flop. **3**

5A. Briefly explain how PLDs are classified. **3**

5B. With diagrams explain different types of FPGA architectures. **4**

5C. Find a minimum-row PLA to implement the following two functions: **3**

$$f(A,B,C,D) = \Sigma m(4,5,10,11,12)$$
$$g(A,B,C,D) = \Sigma m(0,1,3,4,8,11)$$
$$h(A,B,C,D) = \Sigma m(0,4,10,12,14)$$

6A. Explain the different type of programmable interconnects used in FPGAs. **6**

6B. Explain boundary scan test methodology with a block diagram. **4**

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