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# MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

*A Constituent Institution of Manipal University*

## FIFTH SEMESTER B.TECH (INSTRUMENTATION & CONTROL ENGG.)

## END SEMESTER EXAMINATIONS, NOV/DEC 2016

SUBJECT: DIGITAL SYSTEM DESIGN [ICE 311]

Time: 3 Hours MAX. MARKS: 50

**Instructions to Candidates:**

- Answer **ANY FIVE FULL** questions.
- Missing data may be suitably assumed.

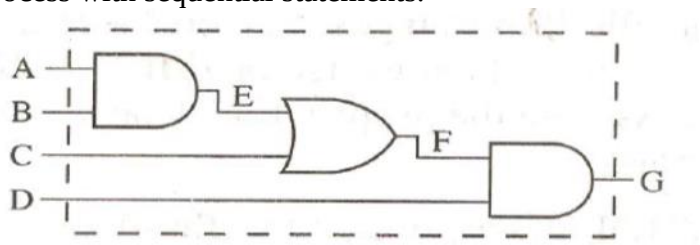
**1A.** Write the truth table for following equation: **3**

$$F = (A \oplus B)C + A'(B \oplus C)$$

**1B.** Write VHDL code for the following circuit. Assume that the gate delays are negligible. **4**

(a) Use concurrent statements.

(b) Use a process with sequential statements.




**1C.** What do you mean by hazards in combinational networks? Explain the types of hazards. **3**

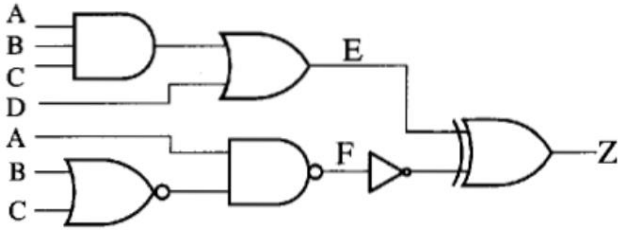
**2A.** Explain the different Scalar data types used in VHDL. Illustrate each with examples. **4**

**2B.** Draw a complete Y-chart showing different levels and domains of abstraction. **3**

**2C.** Explain the structure of a VHDL program. **3**

**3A.** Write a sequential VHDL code for a T flip-flop. **3**

**3B.** Write a VHDL description of the following combinational circuit using concurrent statements. **4**




**3C.** Explain procedures and write a procedure for sorting a greater value when two values are provided. **3**

**4A.** Write a structural VHDL code for a full adder assuming that full adder has been defined as a component. **4**

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| **4B.** | Briefly explain the different operators used in VHDL. | **3** |
| **4C.** | Write a test bench to verify the working of a JK flip-flop. | **3** |
| **5A.** | Briefly explain how ROMs are classified. | **3** |
| **5B.** | Explain the different types of FPGA programming technologies. | **4** |
| **5C.** | Find a minimum-row PLA to implement the following two functions: | **3** |

$$f(A,B,C,D) = \Sigma m(3,4,6,9,11)$$
$$g(A,B,C,D) = \Sigma m(2,4,8,10,12,14)$$
$$h(A,B,C,D) = \Sigma m(3,6,7,10,11)$$

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| **6A.** | With a block diagram explain the operation of a programmable I/O block in FPGA. | **6** |
| **6B.** | Explain scan testing with a block diagram. | **4** |

********** END **********