Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

SEVENTH SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION - NOV/DEC 2016
SUBJECT: LOW POWER VLSI DESIGN (ECE - 429)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ANY FIVE** full questions.
- Missing data may be suitably assumed.

1A. Derive an expression for short circuit power in CMOS inverter and discuss the significance of the expression from the point of view of opportunity for reduction of power.

1B. Disuses DVS and AVS techniques for reducing dynamic power dissipation in VLSI.

(5+5)

2A. Explain i) Segmented Bus architecture and ii) Low swing Bus employed in VLSI to reduce dynamic power.

2B. Describe i) Guarded Evaluation and ii) pre-computation techniques employed in low power designs. Also, using appropriate VHDL coding show how they can be implemented at the RTL level.

(5+5)

3A. Using appropriate example show how Bus invert coding technique can be implemented. What are its salient features? Illustrate with examples.

3B. Estimate the intrinsic wire delay of a Cu wire of length 10mm in 0.13 um CMOS technology, with a thickness 0.3 um, width 0.3 um and height 0.35 um above M1 ground plane with SiO2 dielectric. Assume: resistivity = 24 ohm-um, c = 0.12 fF/um. What will be the delay if a buffer with 150ps delay is inserted at the centre of the line?. What is the overall delay if the line is divided in to 4 segments and buffers of 150ps are inserted?

3C. What are the techniques used to reduce cross talk in interconnects? List.

(5+3+2)

4A. Explain i) Dual Vth technique and ii) Dynamic body biasing technique for reducing the leakage power in VLSI circuit and compare them

4B. Discuss the process level techniques for reducing leakage power in MOSFETs.

(5+5)

5A. Describe the concept of i) Gate-length Biasing and ii) LECTOR for leakage reduction

5B. Discuss the techniques employed for Gate Leakage control in MOSFETs

5C. Assume that the Display in your cell phone has an average transition delay (shut down and wake up) of 5ms, power in sleeping and working state are 5mW and 60 mW respectively. Also the transition energy is of 40 mW-sec. What is the minimum idle time required to consider switching to power down mode?

(5+3+2)

6A. Discuss the DPM policies with their salient features

6B. What are the techniques used while coding to reduce power in processors? Explain with examples.

(5+5)