Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

SEVENTH SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION - NOV/DEC 2016
SUBJECT: LOW POWER VLSI DESIGN (ECE - 429)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ANY FIVE** full questions.
- Missing data may be suitably assumed.

1A. Discuss the hierarchical low power design strategies with their relative impact on power reduction, power estimation accuracy and performance.

1B. What makes pipelining and parallel architectures suitable for low power operation? Explain and compare the two strategies.

(5+5)

2A. List the problems encountered while employing dual V_{dd} technique and suggest remedies to overcome them.

2B. Using appropriate example, show how Dynamic Supply Gating can be implemented. Also explain how it can be extended to any arbitrary logic circuits?

(5+5)

3A. Discuss various clock gating schemes for low power operation. Also, using appropriate VHDL coding show how any one of them can be implemented at the RTL level.

3B. In a certain VLSI chip there are 100 Million transistors, of which, 20 Million are in logic circuits with average width of 10λ and rest of them forms memory circuit with average width of 4λ. Assume 90nm technology, Cg of 2fF/μm and an V_{dd} of 1.2 Volts, the switching factor for the logic circuits is 0.2 and for memory array it is 0.05. Calculate the dynamic power consumption if a clock of 800MHz is employed.

3C. Illustrate the impact of logic restricting and input ordering on the switching activity.

(5+3+2)

4A. Explain power gating technique and with suitable analysis, discuss the design issues related to the footer transistor for implementing power gating.

4B. In a certain chip, a metal 2 wire has 10mm long and 0.32 λ wide. The sheet resistance is 0.05 ohm /□ and the capacitance per micron is 0.2fF/ μm. (Assume 90nm technology).
i) Estimate the delay offered by the wire
ii) If we have to introduce 3 buffers find out optimum delay of the buffer
iii) What is the overall delay after inserting 3 buffers?

4C. List the main sources of leakage power in MOSFETs.

(5+3+2)

5A. Describe the concept of i) Gate-length Biasing and ii) VTCMOS for leakage reduction

5B. Discuss the following:
i) Procrastination Scheduling
ii) Memory optimisation for low power

5C. What is the impact of using repeaters in interconnects? Explain.

(5+3+2)

6A. What are the criteria to be looked at while considering sending a component to sleep state in a system? Obtain an expression for break-even time for such a component to go to sleep state, assuming the standard operating conditions and highlight its significance.

6B. Describe any three coding techniques used to reduce power dissipation.

(5+5)