Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

SEVENTH SEMESTER B.TECH (MECHATRONICS) DEGREE
END SEMESTER EXAMINATION - NOV/DEC 2016
SUBJECT: ADVANCED EMBEDDED SYSTEM DESIGN (ECE – 453)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ANY FIVE** questions.
- Missing data may be suitably assumed.

1A.	Draw a neat diagram of ARM data flow model and explain each functional component.
1B.	Explain the mechanism of 3 stage pipelining in ARM7 processor with an example.
1C.	Discuss four major design rules in RISC design.
	(4+4+2)
2A.	LPC 2129 target board is in ARM state. Write a program to flash all LEDs which are connected to IODIR register starting from P1.08 to P1.27. Use maximum time delay for flashing. Repeat the sequence.
2B.	What are the different types of arithmetic instructions in ARM? Explain each with one example.
2C.	Explain little and big endian memory.
	(4+4+2)
3A.	Consider ARM processor to be in ARM state. How are stack operations carried out in ARM processor? Tabulate all the addressing modes and explain with an example.
3B.	Consider ARM processor to be in ARM state. Write a program to add two 64 bit numbers stored in memory locations pointed by registers r0 and r1. Store the sum in memory location pointed by register r0.
3C.	Explain different types of cache, based on its position between processor and main memory.
	(4+4+2)
4A.	Explain AMBA based system emphasizing on bus transfers, slave, APB, AHB and ARM multiplexed bus scheme.
4B.	a) Using address decoder and other logic circuits interface ARM processor with 2Kx 8 RAM at starting address FFFFF800H b) Using address decoder and other logic circuits interface ARM processor with 4Kx 8 ROM at starting address FFFF6000H
4C.	Discuss ARM address register structure.
	(4+4+2)
5A.	What are the different tasks of MMU? With regard to ARM MMU, explain page tables, page table entries and different types of page table walks.
5B.	Define different types of caches based on its location. With each cache line of 32 bit words, explain architecture of 8 KB unified cache with necessary diagrams.
5C.	Explain Polling I/O strategy with algorithm or sample program used for implementation.

		(4+4+2)
6A.	With a neat block diagram, describe how ARM core is used in an VLSI ruby II Advanced Communication Processor?	
6B.	How Set associativity of cache can be increased using content address memory? Describe using an example and necessary diagram.	
6C.	1.	<u>8 KB I & D cache</u>. Instruction miss rate = 0.64%. Data miss rate = 6.47%. Hit time = 1. Miss time = 50. 90 % accesses are from instructions.
	2.	<u>16KB unified cache.</u> Aggregate miss rate = 1.99%. Hit time = 1. Miss rate = 50. 90 % accesses are from instructions. Which of the above one is better option??
		(4+4+2)