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MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

**SEVENTH SEMESTER B.TECH (MECHATRONICS) DEGREE**
**END SEMESTER EXAMINATION - DEC/JAN 2017**
**SUBJECT: ADVANCED EMBEDDED SYSTEM DESIGN (ECE – 453)**

**TIME: 3 HOURS** **MAX. MARKS: 50**

**Instructions to candidates**
- Answer **ANY FIVE** questions.
- Missing data may be suitably assumed.

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| 1A. | Sketch block diagram of ARM core data flow model and describe the following.<br>i) Barrel Shifter<br>ii) CPSR<br>iii) Register set |
| 1B. | Explain mechanism of 5 stage pipelining in ARM processor with an example. |
| 1C. | Discuss physical features of ARM design philosophy. |
| | (4+4+2) |
| 2A. | ARM state LPC 2129 target board. Write a program to display LEDs is connected to each pins starting from P1.16 to P1.23 of IODIR register. LEDs connected to these pins should be turned on and off one by one with a maximum time delay in between. Repeat the sequence. |
| 2B. | What are the different types of logical instructions in ARM? Explain each with one example. |
| 2C. | What are the different data types ARM supports in high level languages? Explain. |
| | (4+4+2) |
| 3A. | Consider ARM processor to be in ARM state. How multiple load store operations are carried out in ARM processor? Tabulate all addressing modes and explain with an example. |
| 3B. | ARM mode in Thumb state. Write a program to add two 32 bit numbers stored in memory locations pointed by registers r0 and r1. Store the sum in memory location pointed by register r0. |
| 3C. | Explain different types of cache, based on its architecture. |
| | (4+4+2) |
| 4A. | Design a virtual to physical memory mapping scheme with following specifications.<br>Virtual address space = 32 K<br>Main memory size = 8K<br>Page size = 2K<br>Secondary memory address = 24 bits.<br>Main memory frame = 2 bits<br>Future = 5 bits<br>Resident bit = 1<br>Virtual address issued = 011100000101011. |
| 4B. | Explain AMBA based system emphasizing on bus transfers, slave, APB, AHB and ARM multiplexed bus scheme. |

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| 4C. | Discuss pointer arithmetic and conditional statements used as architectural support for high level languages in ARM. |
| | (4+4+2) |
| 5A. | Define MMU. With regard to ARM MMU, explain the following, with necessary diagrams.<br>i) Page and Page frame<br>ii) Mapping of Virtual memory to Physical memory for single region.<br>iii) Mapping of Virtual memory to Physical memory for three regions (single task) with the usage of page tables.<br>iv) Mapping of Virtual memory to Physical memory for multiple tasks with the usage of page tables. |
| 5B. | How Set associativity of cache can be increased using content address memory?<br>Describe using an example and necessary diagram. |
| 5C. | Explain Interrupt I/O strategy with algorithm or sample program used for implementation. |
| | (4+4+2) |
| 6A. | With block diagram, describe how ARM core is used in an Ericsson –VLSI blue tooth base band controller? |
| 6B. | Describe different privileged and non- privileged processor modes in ARM. Also highlight importance of banked registers during interrupts / exceptions. |
| 6C. | Discuss different factors affecting cache optimization and solutions to overcome them. |
| | (4+4+2) |