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INTERNATIONAL CENTRE FOR APPLIED SCIENCES

(Manipal University)

III SEMESTER B.S. DEGREE EXAMINATION – APRIL / MAY 2017

SUBJECT: COMBINATIONAL AND SEQUENTIAL LOGIC (EC 231)

(BRANCH: CS, CE, E&C and E&E)

Tuesday, 16 May 2017

Time: 3 Hours **Max. Marks: 100**

- ✓ **Answer ANY FIVE full Questions.**
- ✓ **Missing data, if any, may be suitably assumed**

1A. Consider a logic circuit having 3 inputs A, B, C and 2 outputs Y1 and Y2 given by $Y1 = \sum m\,(1,2,4,7)$ and $2 = \sum m(3,5,6,7)$.

i) Write the truth table of the circuit.
ii) Simplify Y1 and Y2 using K-map.
iii) Implement Y1 and Y2 using AOI Logic.
iv) Identify function of the circuit.

1B. Perform the following subtraction using 2's compliment method.

i) $(01000)_2$ - $(01001)_2$ ii) $(0011.1001)_2$ -$(0001.1110)_2$

1C. Minimize the logic function $Y(A,B,C,D) = \sum m(1,3,5,8,9,11,15) + d(2,13)$. Use Karnaugh map and draw simplified logic circuit using only NAND gates.

1D. Obtain the set of prime implicants for the Boolean expression $F = \sum m(0,1,6,7,8,9) + d(13,14,15)$ using Quine-McCuskey method **(4+4+4+8)**

2A. Implement the Boolean function F (A, B, C, D) = $\sum m(0,3,4,5,8,9,11,12,13)$ using

a) 8 to 1 Multiplexer and basic gates.
b) 4 to 1 Multiplexer and basic gates.

2B. Draw the circuit diagram of a Master-slave J-K flip-flop using NAND gates. What is race around condition? How is it eliminated in a Master –slave J-K flip-flop?

2C. What is synchronous counter? Design a Mod-5 synchronous up counter using J-K Flip-Flops.

2D. List the distinguishing factors of ROM, PROM, EPROM, and EEPROM. **(4+5+6+5)**

3A. Implement 8421 BCD to Excess-3 converter using 3 to 8 decoders.

3B. Represent the following numbers in 8-bit binary form.

a) $(-43)_{10}$
b) $(-200)_{10}$
c) $(+125)_{10}$
d) $(AF)_{16}$
e) $(-225)_{10}$

3C. Construct a mod 11 ripple up counter using negative edge triggered JK Flip-Flops. Draw the timing diagram.

3D. Write behavioral VHDL code for 4 bit binary to gray code converter. **(5+5+6+4)**

4A. Explain the working of a 4-bit PISO shift registers. Draw the timing waveforms

4B. Write the truth table of SR and D flip flops. Using S-R flip flop show how a D flip flop can be realized.

4C. With the help of truth table and state diagram draw the logic diagram for a 4-bit ring counter and Johnson counter using D flip flops also sketch the timing waveforms.

4D. Write a structural VHDL code for a two binary adder using full adders. **(5+5+5+5)**

5A. Design a sequential circuit using D flip-flop, to generate the following sequence 1,3,5,2,4,1,3,5,2,4…….Assume that no invalid states occur.

5B. Derive the characteristic equation for SR, JK D and T Flip-Flops.

5C. Write the syntax for the following terms with respect to VHDL

a) Entity and architecture declaration b) case and process statements

5D. Implement the following Boolean functions using PAL with 4 inputs and 3-wide AND-OR structure.

F1= $\sum m(2,12,13)$

F2= $\sum m(0,2,3,4,5,6,7,8,10,11,15)$ **(5+5+4+6)**

6A. A combinational circuit has 3 inputs A, B and C and an output F. The output F is true only for the following input combinations:

A is false and B is true
A is false and C is true
A, B and C are all false
A, B and C are all true

a) Write the truth table for F.
b) Write the simplified expression in SOP form.
c) Draw a logic circuit implementation for F using the minimum number of 2 input NAND gates only.

6B. Design a mod 6 synchronous up counter using JK Flip flops.

6C. Implement the functions $F1(a,b,c) = \prod(0,1,5,6,7)$ and $F2(a,b,c) = \sum(1,2,4,6,7)$ using 3 to 8 decoder and minimum input OR/NOR gates.

6D. State and prove Demorgan's Theorem. Prove that NAND gate is a Universal gate.

(5+5+5+5)

7A.Convert the following numbers to the specified Base:

a) $(B9F.AE)_{16}$ = (?)$_8$
b) $(2598.675)_{10}$ = (?)$_{16}$
c) $(378.93)_{10}$ = (?)$_8$
d) $(AOF9.0EB)_{16}$ = (?)$_{10}$
e) $(4433)_5$ = (?)$_{10}$

7B. Derive a logic expression that is true only when the two binary numbers A1, A0 and B1, B0 have the same value. Draw the logic diagram using only NOR gates.

7C. Perform the following decimal subtractions in BCD by the 9's compliment method.
a) 305.5 – 168.8 b) 679.6 – 885.9

7D. Reduce the following expression using Boolean laws:
$a) F1 = A + B[AC + (B + C')D]$ b) $F2 = (B + BC)(B + B'C)(B + D)$ **(5+5+5+5)**

8A. Design and implement 3 bit odd parity generator and checker circuit.

8B. Design a 2 bit magnitude comparator using AOI Logic. Write dataflow VHDL code for 2 bit magnitude comparator

8C. Design an octal to binary encoder using basic gates.

8D. Design a combinational circuit to produce 2's compliment of a 4 bit binary number and Realize using logic gates. **(5+5+5+5)**