Reg.No.									

INTERNATIONAL CENTRE FOR APPLIED SCIENCES

(Manipal University)

IV SEMESTER B.S. DEGREE EXAMINATION – APRIL/ MAY 2017

SUBJECT: COMPUTER ARCHITECTURE (CS 242)

(BRANCH: CS &CE)

Thursday, 4 May 2017

Time: 3 Hours **Max. Marks: 100**

- ✓ **Answer ANY FIVE full Questions.**
- ✓ **Missing data, if any, may be suitably assumed**

1A. i. Explain the computer components with diagram.
ii. Define interrupt. Explain different classes of interrupts.

1B. With neat diagram explain the instruction cycle state diagram with interrupts.

(10+10)

2A. Consider an address space of 16MB. The memory space is specified by 20 bits. If the page no. field of the virtual address is 10 bits, find the following:
i. No. of bits needed to specify the address space
ii. Size of the memory space
iii. Size of a page
iv. No. of pages
v. No. of blocks

2B. i. Write short notes on magnetic read and write mechanisms of auxiliary memory with diagram.
ii. Define cache memory. With neat diagram explain associative mapping. Also write the advantages and disadvantages of associative mapping.

(5+15)

3A. Explain the following:
i. Mapping logical address in to a physical address in segmented paging with diagram.
ii. The basic components of memory management hardware unit.

3B. Explain the various types of instruction set operations.

(8+12)

4A. i. Explain Pentium address translation mechanism with diagram.
ii. Explain Power PC addressing modes with diagram

4B. i. Explain different categories of user visible registers of CPU.
ii. With neat diagram explain single address field sequencing technique in the case of micro instruction.

(10+10)

5. Explain the micro operations for the following:
   i. Fetch cycle
   ii. Indirect cycle
   iii. Execute cycle
   iv. Instruction cycle

(6+6+4+4)

6A. i. Explain the algorithm of finding the 2's complement division. Divide (-7)/3 using this algorithm.
   ii. Represent the following in 32-bit IEEE 754 floating point format.
      a) 3.75
      b) -1/32

6B. With neat diagram explain the Overlapped register windows in Berkley RISC processor.

(12+8)

7A. Explain the strobe control method of asynchronous data transfer.

7B. i. What is delayed branch in RISC pipeline? Explain
   ii. To perform arithmetic operation (Ai+Bi)(Ci+Di) for i=1,2,3,4,5,6, draw the pipeline configuration. List the content of all the registers in the pipeline for the different values of i.

(10+10)

8. Write short note on:
   a) SISD
   b) MIMD
   c) CISC characteristics and RISC characteristics
   d) Multiplication of floating point numbers
   e) Parallel arbitration logic

(5 x 4)