Reg. No.										

INTERNATIONAL CENTRE FOR APPLIED SCIENCES

(Manipal University)

IV SEMESTER B.S. DEGREE EXAMINATION – APRIL / MAY 2017

SUBJECT: VLSI DESIGN (EC 245)

(BRANCH: E & C)

Saturday, 29 April 2017

Time: 3 Hours **Max. Marks: 100**

- ✓ **Answer ANY FIVE Questions.**
- ✓ **Layout must be drawn using the graph sheet provided.**
- ✓ **Missing data may be suitably assumed.**

1A. Given that 1□Cg = 0.01pF.

i) Find the optimal number of NMOS inverters to be cascaded so as to drive an off-chip capacitive load of 1.48pF such that the total delay is minimized.

ii) Give the cascaded structure, clearly showing the L:W ratios.

iii) Show the delay T_d across each inverter stage and hence calculate the overall delay.

1B. Explain the working of 6T- SRAM cell in detail.

1C. Show that the super buffer circuit is used to overcome the unequal rise and fall time in NMOS inverters? Give both the configurations of super buffer.

(10+5+5)

2A.What is a cross-bar switch? Bring out the differences between barrel shifter and cross-bar switch. Give the circuit implementation and the stick notation of 4X4 barrel shifter.

2B.The NMOS transistors in the circuit of **FIG. 2B** have $V_t = 1V$, $\mu_n C_{ox} = 120\ \mu A/V^2$ and L1=L2=L3= 1µm. Find the required values of gate width for each of Q1,Q2 and Q3 to obtain the voltage and current values indicated. **(10+10)**

3A. Compare BJT and MOSFET with respect to following parameters:
(i) Transconductance value (ii) Input impedance (iii) Noise (iv) Ease of integration and fabrication (v) Current handling capability

3B. Show that the inverter pair delay using two identical pseudo-NMOS inverters is larger by a factor 1.7 than that using minimum size NMOS inverters with depletion-mode pull-up.

3C. Derive the expression for rise time and fall time in a CMOS inverter. **(5+5+10)**

4A. Explain the lambda based design rule for i) Wires (nMOS and CMOS) ii) Transistors (NMOS, PMOS and CMOS).

4B.Find the region of operation for NMOS based circuits given in **FIG.4B**. Assume $V_T = 0.4V$. **(10+10)**

5A. In the inverter circuit: what· is meant by Zp.u. and Zp.d.? Derive the required ratio between Zp.u. and Zp.d. if an nMOS inverter is to be driven from another nMOS inverter.

5B. Explain in detail about working of MOS capacitor.

5C.What do you understand by channel length modulation? Explain in detail. **(10+5+5)**

6A.Explain the following terms in detail:

i) Back gate effect ii) Mobility variation iii) Fowler-Nordheim tunnelling
iv) Drain Punchthrough v) Impact Ionization-Hot electrons.

6B. Calculate the effective input capacitance for the given multi-layer structure in **FIG. 6B** for 5µm process. Relative Capacitance value for metal1= 0.075, polysilicon=0.1 and Gate to channel = 1.0. **(10+10)**

7A. Explain the principles of photo lithography. Discuss the working of positive photo resist and negative photo resist with necessary diagrams.

7B. For a CMOS Inverter having$L_n = L_p = W_n = 1.2$ µm, $W_p = 5$ µm .Compute the following: (i) rise timet_r (ii) fall-timet_f (iii) total delay $T_d$through a pair of inverters. Given the typical sheet resistance and standard capacitance values for 1.2 µm process [i] NMOS channel resistance = 20 kΩ/square [ii] PMOS channel resistance = 45 KΩ /square[iii] Gate-to-channel capacitance = 16pF x 10^{-4}/um^2.

7C. With neat figures explain the different steps involved in the fabrication of PMOS transistor. What is the advantage of self-aligned process? **(5+5+10)**

8A. Draw the circuit, stick diagram and layout for two input NMOS NOR gate.

8B. Implement
i) 2 input NAND function using a) pass transistors, b) Transmission gates.
ii) 2 input NOR function using a) NMOS logic with depletion load, b) CMOS logic **(10+10)**

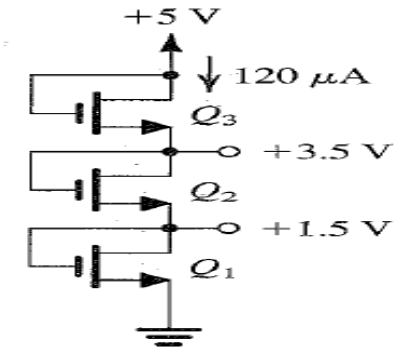
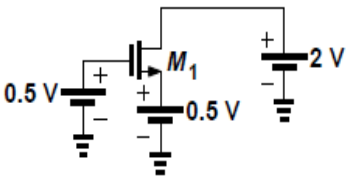
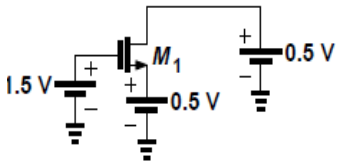


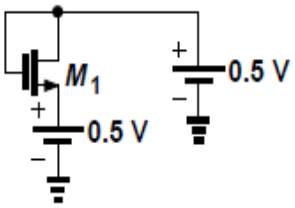
FIG. 2B



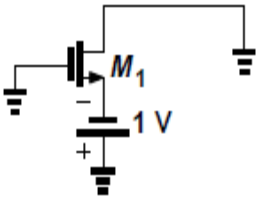
(i)



(ii)



(iii)



(iv)

FIG.4B

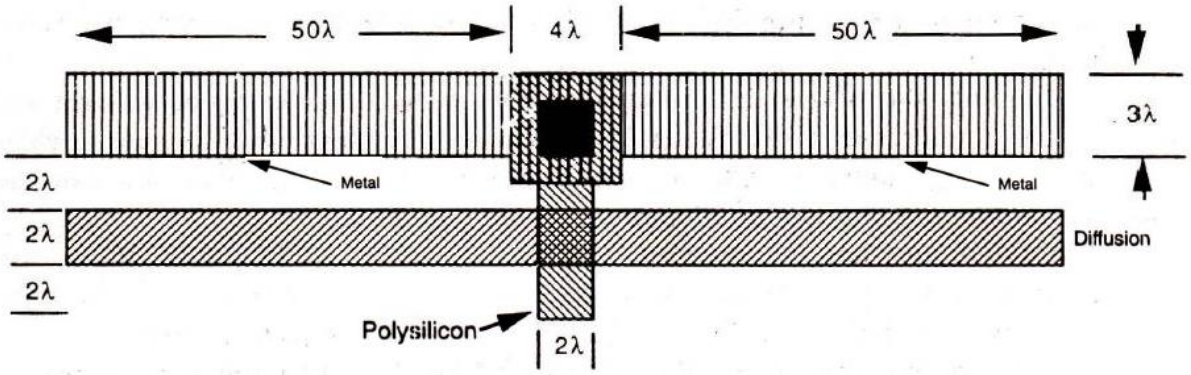


FIG. 6B