Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

SECOND SEMESTER B.Tech. (E & C) DEGREE END SEMESTER EXAMINATION - April/May 2017

SUBJECT: BASIC ELECTRONICS (ECE - 1001)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A.	Consider the fixed bias circuit of n-p-n transistor. If V_{cc} = 12V, R_B =240kΩ, R_c= 2.2kΩ and β =50 i) Draw the circuit. ii) Determine the values of V_{CE}, I_B and I_C iii) Draw the DC load line.
1B.	Draw the circuit of NPN transistor in common base configuration. Plot and explain its input - output characteristics
1C.	Distinguish between Zener breakdown and Avalanche breakdown. Draw the V-I characteristics of Zener diode under reverse bias condition.
	(5+3+2)
2A.	An AC supply of 230V, 50Hz, is applied to a centre-tapped full wave rectifier circuit through transformer of turns ratio 10:1. Draw the circuit diagram. Assume diode forward resistance as 10Ωs, and the cut-in voltage is zero. If the load resistance is 1000Ωs, calculate: (i) dc current flowing through the load, dc voltage across the load, dc power delivered to the load, ac input power, ripple voltage across the load and its frequency, (ii) the capacitor value of a filter to remove 99% of the ripple of this rectifier.
2B.	Draw the Zener voltage regulator with R_s=220Ω,V_z=20V,I_{zmax} = 60mA and R_L=1.2KΩ. Determine the range of values of Vi that will maintain the Zener diode in the ON state.
2C.	Compare the response of RC coupled amplifier with and without feedback.
	(5+3+2)
3A.	For an op-amp square wave generator circuit determine R for the following given specifications. Frequency of oscillation = 8 kHz, output voltage $V_{0\ (p\text{-}p)}$ = 10 V, Capacitor C = 0.01μF, R_1 = R_2. Draw the circuit diagram and related waveforms.
3B.	Derive the general expression for the output of op-amp difference amplifier circuit with V_1 and V_2 as the inputs. Determine the component values to get an output $V_0 = 3V_2 - 2V_1$ for this circuit.
3C.	In the circuit shown in FIGURE.Q3C, calculate the output voltage V_0 when (a) $V_1 = V_2 = 0.2$ V (b) V1 = V2 = 1V
	(5+3+2)

4A.	i) Subtract $(36.25)_{10}$ from $(75.75)_{10}$ using 1's complement. ii) Design a combinational logic circuit which performs the addition of three bit binary numbers. Obtain simplified expression for the system using K map and implement it using basic gates.
4B.	With a neat logic diagram explain the shifting of data 11010 (The right most bit is LSB which enters first) in Serial-in Serial-out 4-bit shift right register. Also mention how many clock cycles are required to shift the MSB of the above mentioned data to the output.
4C.	Draw the circuit diagram of SR flip-flop using NAND gates and write the truth table for the same.
	(5+3+2)
5A.	Certain AM transmitter radiates 9kW of power with carrier unmodulated and 10.125kW of power when carrier is sinusoidally modulated. Calculate the modulation index. If another sine wave corresponding to 40% modulation is transmitted simultaneously, determine the total power radiated.
5B.	Draw the waveform of different types of pulse modulated signals considering sinusoidal signal as a message and train of pulses as carrier.
5C.	Mention the different types of network topologies and compare them.
	(5+3+2)

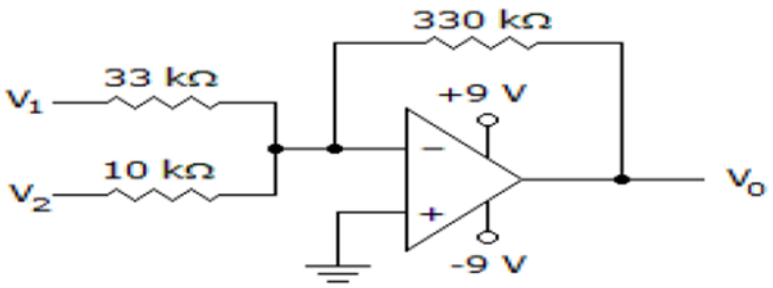

FIGURE Q3C