Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

SECOND SEMESTER B.TECH DEGREE END SEMESTER EXAMINATION - APRIL / MAY 2017

SUBJECT: BASIC ELECTRONICS (ECE - 1001)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Obtain the expression for base current in case of self-bias circuit for n-p-n transistor and show that collector current is independent of β.

1B. Draw the circuit of NPN transistor in common emitter configuration. Plot and explain its input - output characteristics.

1C. A Ge diode for which the reverse saturation current is 5μA has a forward current of 100 mA at 27^0C. Calculate the forward voltage drop across it.

(5+3+2)

2A. Draw the diagram of bridge rectifier circuit. An ac supply of 230V, 50Hz, is applied to this circuit through transformer of turns- ratio 11:1. Assume diode forward resistance as 10Ω, and the cut-in voltage as zero. If the load resistance is 500Ω, calculate: (i) dc current flowing through the load and dc voltage across the load. ii) dc power delivered to the load. iii) ac input power. iv) Ripple voltage across the load and its frequency. (v) The capacitor value of a filter to remove 99% of the ripple of this rectifier.

2B. Draw the Zener voltage regulator circuit. Given that V_i=50V, R_s=1KΩ, V_z=10V, I_{zmax}=32mA, determine the range of load resistance and load current that will result in load voltage being maintained at 10V.

2C. Draw the circuit diagram of RC coupled amplifier and its frequency response. What is the need of capacitor coupling in amplifiers?

(5+3+2)

3A. Design the circuit using op-amps to provide the output as

$$V_0 = 2V_1 - 3V_2 + 4V_3 - 5V_4$$

(V_1,V_2,V_3 and V_4 are the inputs to the circuit.)

3B. Draw the circuit of inverting OPAMP integrator. With R= 1KΩ, C= 1μF and $\pm V_{SAT}$ = 12V, determine the magnitude of the output voltage if the input is square wave of frequency 1KHz as shown in FIGURE Q3B.

3C. An Op-amp has inputs V_1 = 10 mV and V_2 = 8mV. If the differential gain is 60 dB and CMRR is 80 dB, calculate differential output voltage and common mode output voltage.

(5+3+2)

4A. i) Perform $(143.76)_8 + (72.62)_8 = (\ ?\ )_8$

ii) Reduce the expression $f = A[B + C'(AB + AC')']$ using Boolean laws.

iii) Consider a logic system with four inputs A, B, C and D that will produce output '1' whenever two or more adjacent input variables are 0's.(A and D are also to be treated as adjacent). Obtain simplified expression for the system using K map and implement it using minimum number of NAND gates only.

4B. Realize a 3-bit up counter using positive edge triggered JK flip flops. Draw the timing diagram for the same.

4C. Explain the working of NOR gate using discrete components.

(5+3+2)

5A. A message signal $10\sin(2\pi \times 10^3 t)$ is used to amplitude modulate a carrier signal $25\sin(2\pi \times 10^5 t)$. Determine the modulation index, frequency of the sideband components with their amplitudes and power delivered to 500Ω load. What is the bandwidth of the modulated signal?

5B. Draw the modulated signal using ASK, FSK and PSK modulation techniques for the digital message 10110.

5C. List and briefly explain multiple access techniques used in digital communication.

(5+3+2)

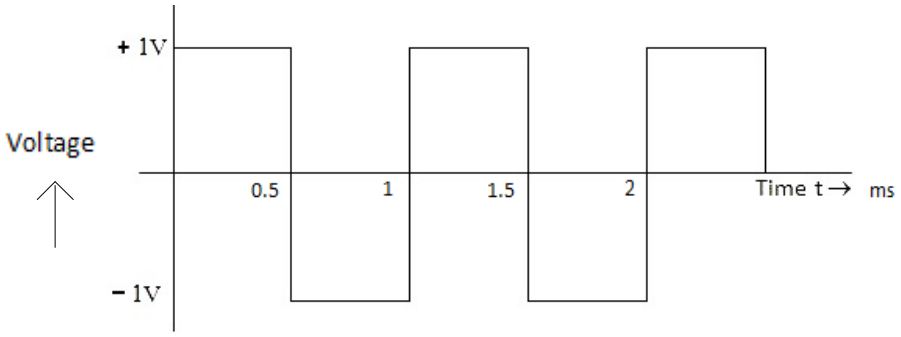

FIGURE Q3B