Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
A Constituent Institution of Manipal University

IV SEMESTER B.Tech. (BME) DEGREE MAKE-UPEXAMINATIONS, JUNE 2017

SUBJECT: DIGITAL SYSTEM DESIGN (BME 2203)
(REVISED CREDIT SYSTEM)
Monday, 19th June 2017: 2 to 5 PM

TIME: 3 HOURS **MAX. MARKS: 100**

Instructions to Candidates:

1. **Answer ALL questions.**
2. **Draw labeled diagram wherever necessary**

1.	(a)	With a neat diagram explain operation of CMOS inverter gate.	06
	(b)	What are Semi customized Application Specific Integrated Circuits? Explain with an example?	06
	(c)	Design a two input CMOS based NAND gate and explain.	08
2.	(a)	What is TOP-DOWN approach of digital system design? Explain.	06
	(b)	Draw the diagram of a latch using transmission gates and explain its operation.	06
	(c)	Design a full adder using PLA (Programmed Logic Array), draw the diagram of AND-OR planes and explain.	08
3.	(a)	What is Configurable Logic Block (CLB)? Draw architecture of FPGA using CLBs and explain.	07
	(b)	Define Shannon's expansion theorem. Expand the following logic function with the help of Shannon's co-factors, for a given w_1: $f = \bar{w_1} w_3 + w_2 \bar{w_3}$. Draw the synthesized circuit using 2 to 1 MUX.	07
	(c)	Implement the function $f = \bar{w_1} w_3 + w_2 \bar{w_3}$ using 2 input LUTs.	06

4. (a) Explain an architecture of a simple PLD device. 07

(b) Explain the design of Verilog HDL module for implementing a "2 bit adder" circuit. 08

(c) Explain the generation of a waveform in Verilog HDL using "initial" statement. 05

5. (a) Explain the usage of statement "always" in *blocking style*. 06

(b) Design a Verilog HDL module for the "2 to 1 Multiplexer" (in behavioral style) and draw the associated hardware details. 07

(c) Describe the design of an "N x N" bit multiplier using combinational units. 07