Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
A Constituent Institution of Manipal University

IV SEMESTER B.TECH. (BME) DEGREE END SEM EXAMINATIONS APRIL/MAY 2017

SUBJECT: DIGITAL SYSTEM DESIGN (BME 2203)
(REVISED CREDIT SYSTEM)
Wednesday, 26th April 2017, 2 to 5 PM

TIME: 3 HOURS **MAX. MARKS: 100**

Instructions to Candidates:

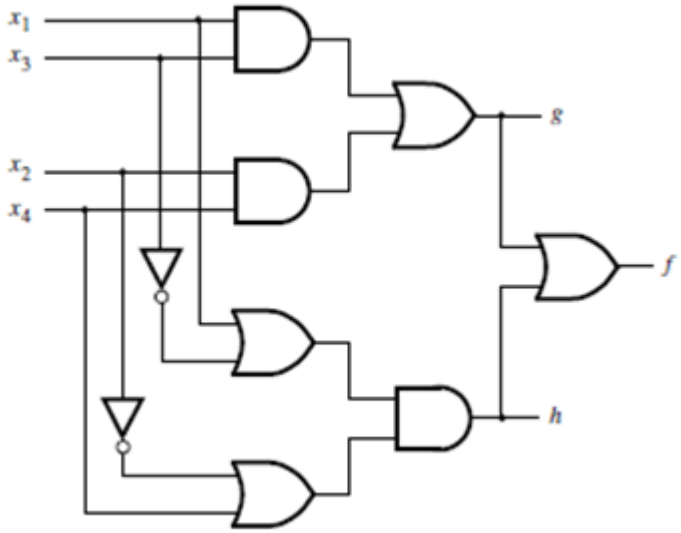
1. **Answer ALL the questions.**
2. **Draw labeled diagram wherever necessary**

1.	(a)	Explain the acceptable logic "high" and logic "low" levels of CMOS.	04
	(b)	Design a two input CMOS based OR gate, and describe the details of each of the transistors and their operation. Verify the truth table associated with the circuit, with the help of transistor ON/OFF state.	06
	(c)	Explain the "TOP-DOWN" approach to design a digital system. Draw a neat labelled diagram of the "Y chart", and explain.	10
2.	(a)	How is a *Fully customized Application Specific Integrated Circuit (ASIC)* different from a *Semicustom ASIC*?	06
	(b)	Explain the functioning of transmission gate as a switch, and describe how it can be used in the design of a non- inverting buffered multiplexer.	06
	(c)	Design a 2 to 4 decoder using nMOS-based PLA (Programmed Logic Array), and draw the diagram of AND-OR planes.	08
3.	(a)	Explain the general architecture of FPGA and discus the improvement, it provides over CPLD architecture.	08
	(b)	Expand the following logic function with the help of Shannon's co-factors, for a given w_2 in the function: $f = w_1w_2 + w_1w_3 + w_2w_3$. Draw the synthesized circuit using 2 to 1 MUX.	06
	(c)	Draw the diagram of a 2 input LUT. Implement the function $f = w_1w_2 + w_1w_3 + w_2w_3$, using 2 input LUTs.	06

4. (a) List the major design stages considered for implementing a typical digital system design using FPGA. 06

(b) Draw the simplified architecture of PAL22V10, and describe its major functioning units. 08

(c) Design a Verilog module for the logic circuit given in figure 4 (c) using continuous "assign" statements.



06

Figure 4(c)

5. (a) Draw a neat diagram of the basic unit of SRAM switch, and explain. 06

(b) Design an appropriate Verilog HDL module to describe two cascaded D-FF (use non-blocking style). 08

(c) Write a Verilog HDL module and draw the associated hardware details for the *Full adde*r (design in behavioral style). 06