Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
A Constituent Institution of Manipal University

IV SEM B.Tech (BME) DEGREE END-SEMESTER EXAMINATIONS, APRIL/ MAY 2017.

SUBJECT: INTEGRATED CIRCUIT SYSTEMS (BME 2202)
(REVISED CREDIT SYSTEM)
Friday, 21st April, 2017, 2 to 5 PM

TIME: 3 HOURS **MAX. MARKS: 100**

Instructions to Candidates:

1. Answer ALL questions.
2. Draw labeled diagram wherever necessary

1A) (i) Draw the schematic diagram of an ideal inverting Op-Amp with a voltage shunt feed-back impedance Z *and* Z^1. Describe the virtual ground model for calculating the closed loop gain. 3+5

(ii) For the Op-Amp in (i), assume finite values of A_v and R_i and nonzero R_o, draw the equivalent circuit and obtain the expression of the closed loop gain.

1B) With appropriate circuit diagrams, explain how input resistance R_i and output resistance R_o associated with an Op-Amp can be calculated practically. 3+3

1C) For circuit shown in Fig. Q1C, obtain the expression for V_O. 6

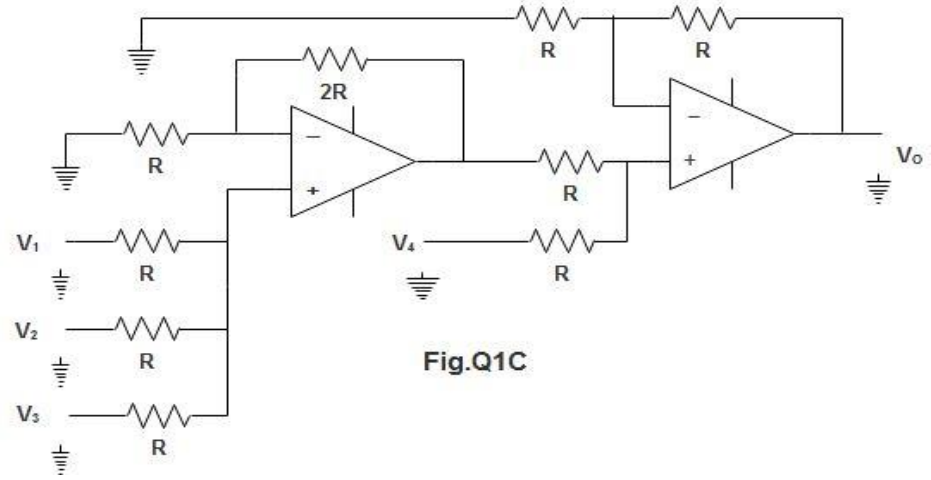

Fig.Q1C

2A) Draw the circuit of a function generator using Op-Amp to generate a square wave and a triangular wave. Explain the operation of the circuit and derive the expression for the time period T associated with the waveforms. 8

2B) Design an inverting Schmitt trigger circuit using an Op-Amp with the following specifications. UTP = 4 Volts and LTP = 2 Volts. Assume that the supply voltage is ± 12 Volts. 6

2C) Draw the circuit of an instrumentation amplifier using Op-Amp, suitable for amplifying the signals from a bridge transducer. Explain its operation. 6

3A) Design and draw the circuit pertaining to a 3rd order band pass Butterworth filter suitable for acquired ECG signal to pass between the frequency ranges of 10 Hz to 200 Hz. The overall gain of the filter is 100. Given, the Butterworth polynomial is $(s+1)(s^2+s+1)$. Sketch the frequency response indicating the gain in dB, f_{OL}, f_{OH} and slope of the fall in gain. 8

3B) Draw the prototype delay equalizer circuit. Derive the expression for the voltage gain A_V. In what condition does this circuit behave as an all pass filter? 6

3C) Draw the pin diagram and the internal circuit diagram of the timer IC. Explain the function of each pin of the IC. 6

4A) Design suitable circuits using timer IC to generate the following waveforms V_{O1} and V_{O2}, shown in Fig. Q4A. 8

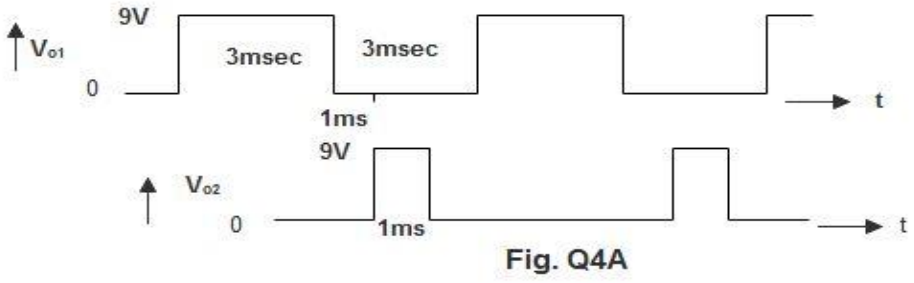

Fig. Q4A

4B) Draw the circuit of a voltage to frequency converter using a timer IC. Derive the expression for the frequency f. 6

4C) With a suitable diagram explain the operation of a 4 bit successive approximation type ADC. Mention its merits and demerits. 6

5A) Design and draw a regulated power supply using IC LM 317 to meet the following specifications. Output voltage can be varied between 12 to 15 volts at a maximum load current of 300 mA. Input is 230 volts 50 Hz ac. Assume the ripple factor to design unregulated supply to be 10%. Use a full wave bridge rectifier and calculate the required specifications of the transformer. 8

5B) With a suitable circuit, explain the operation of a 4 bit binary weighted DAC. 6

5C) Draw the circuit of voltage controlled oscillator using VCO IC 566. If +V=12 volts, R_1=12KΩ, C_1=0.005μF, voltage divider resistors R_2=2KΩ and R_3=10KΩ. Determine the VCO frequency f_O. 6