Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

IV SEMESTER B.TECH. (COMPUTER SCIENCE AND ENGINEERING)

MAKEUP EXAMINATIONS, JUNE 2017

SUBJECT: MICROPROCESSORS [CSE 2203]

REVISED CREDIT SYSTEM
(19/06/2017)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitable assumed.

1A. Draw the internal architecture of 8086 microprocessor and explain the functions of all the components in the unit which is responsible for transfer of data and addresses on the buses. **3M**

1B. Describe the following 8086 instructions with syntax and one numerical example for each. State the flags that are effected in each instruction **5M**

i) AAD ii) LODSB

1C. a) Identify the addressing modes in the following instructions with respect to destination.

i) MOV [SI+5], AX ii) MOV [BX], CL

b) If BX = 0158H, SI = 10A5H, DS = 2100H, CS = 5000H, what is the Effective Address and Physical Addresses for the addressing modes identified in part (a). **2M**

2A. Write a complete 8086 program to accept a string from the keyboard and check if it is a palindrome or not. Display appropriate messages on the screen. **3M**

2B Explain the stack operation with stack diagram during near and far CALL, RET instructions execution. **2M**

2C i) Describe the response that an 8259A will make if it receives an interrupt signal on its IR3 and IR5 inputs at the same time. Assume fixed priority for IR inputs and assume that IR3 and IR5 are unmasked.

ii) What response will the 8259A make if it is servicing an IR5 interrupt and an IR3 interrupt signal occurs? Explain for the following two cases

a) 8086 INTR input was not enabled in IR5 procedure.

b) 8086 INTR input was enabled in IR5 procedure. **5M**

3A. Explain the following signals of 8086 for the minimum mode

a) ALE b) $\overline{WR}$ c) $\overline{RD}$ d) $\overline{DEN}$
e) HLDA f) HOLD g) DT / $\overline{R}$ h) M / $\overline{IO}$ **4M**

3B. With a neat block diagram, explain how logical address is translated to physical address in segment based virtual memory of 80286 processor. **4M**

3C. Describe the enhancements in Pentium Pro compared to Pentium microprocessor. **2M**

4A. Explain the paging mechanism of the microprocessor in which the segments can be as large as 4GB. **5M**

4B. Write a complete assembly language program to count the prime number present in an array of words. Declare the array in the data segment. Store the prime numbers in another array in the memory. Also store the count in the memory. **3M**

4C. What is the difference between the level 2 cache in the Pentium II and the Pentium pro? Explain. **2M**

5A. Explain the following:

a) Bus arbitration and burst control signal groups of 80486
b) Memory system in Pentium processor. **(3+2)M**

5B. Compare hyper-threading to dual processing. **2M**

5C. Consider the following delay loop.

```
        MOV CX,  n1              ; 4Clock Cycles
Outer:  MOV BX, n2               ; 4Clock Cycles
Inner:  DEC BX                   ; 2Clock Cycles
        JNZ  Inner               ;16 or 4 Clock Cycles
        LOOP  Outer              ;17 or 5 Clock Cycles
```

Find the values of n1 and n2 to produce a total delay of 100 milliseconds on an 8086 with 5Mhz clock frequency, if the inner loop gives a delay of 1 millisecond. Show all the steps of your calculation. **3M**