Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

IV SEMESTER B.TECH. COMPUTER SCIENCE AND ENGINEERING

END SEMESTER EXAMINATIONS, APRIL 2017

MICROPROCESSORS[CSE 2203]

REVISED CREDIT SYSTEM
26/04/2017

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. List the purpose of various control flags in 8086 flag register and write how control flags are different from conditional flags. Write the sequence of instructions that will disable single step execution of the program. **3M**

1B. Assume the contents of various segment registers and index registers in hexadecimal is as follows. CS: IP = 348A:1211, SS:BP=2146:1BCA, DS:SI = 3800:1234,DS:DI= 3800:1546 and DS:BX=3800:1856.Write the addressing mode for the source operand and calculate the physical address in hexadecimal for the byte/word read in each of the following instructions given below. **4M**

a) ADD CX,50[BX+SI]
b) SBB BX, [SI+1000H]
c) MOV AX,[BX]
d) CMP CX,[BP+12+DI]

1C. Write a single 8086 instruction that performs each of the following operations. Assume that the values will change in the specified bit positions only and values in the rest of the bit positions will remain the same for each operation. **3M**

a) Sets the rightmost four bits of AX;
b) clears the leftmost three bits of AX;
c) Inverts bits 7, 8, and 9 of AX.

2A. Write an 8086 assembly language program that uses a procedure to combine two strings as given below. Get the two given input strings from the console, pass them as parameters to the procedure and display the resultant string in the console. Assume the two words in the resultant string are separated by a single space. **5M**

String1: Good Morning String2:Best Tactics
Resultant String : GBoeosdt MToarcntiincgs

2B. Explain the following string instructions with an example. **3M**

a) SCAS b) REP MOVSB

2C. Assuming the clock frequency of 8086 as 8MHZ, calculate the value of "N" in the below program to generate a delay of 500µsec. Show the calculations required. **2M**

Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
A Constituent Institution of Manipal University

```
                        Clock Cycles
        MOV CX, N       ; 4
        NOP             ; 3
DO:     NOP             ; 3
        NOP             ; 3
        LOOP DO         ; 17 or 5
```

3A. Assume MN/MX' pin of 8086 is connected to +5V and is ready to perform a read operation from a peripheral input device which has a low data transfer rate. Suppose 8086 takes half of a normal bus cycle in addition to read data from the input device, draw a neat timing diagram to illustrate this case. **4M**

3B. Draw the flowchart for initialization of 8259A Priority Interrupt Controller .Write the values for the following command words when the slave 8259A is connected to IR4 input of master 8259A.Assume IR2 and IR4 of master 8259A has enabled. **4M**
a) ICW3 for the master and ICW3 for the slave.
b) OCW1 for the master 8259A.

3C. Write the control words required to initialize the 8255A Programmable Peripheral Interface as follows: **2M**
a) Port B and upper Port C – input ports, Port A and lower Port C –output ports. All ports in mode 0.
b) Set PC5 of Port C.

4A. With a neat diagram, explain how 24-bit physical address is generated in 80286 protected mode. Also write any two differences between real mode and protected mode operation of 80286. **5M**

4B. State the need of virtual mode in 80386 microprocessor. Also discuss the following signal groups of 80386 processor. **5M**
a) Coprocessor Signaling b) Bus Cycle Definition c) Bus Arbitration

5A. Compare and contrast the memory system in Pentium and Pentium Pro microprocessors. Explain the role of Instruction Fetch and Decode Unit and Retire Unit in Pentium Pro. **3M**

5B. Discuss the following signals of 80486: **2M**
a) $\overline{BE3}$-$\overline{BE0}$ b) $\overline{IGNNE}$ c) $\overline{BS16}$ d) $\overline{PLOCK}$

5C. Explain the following features of Pentium4 and Core 2. **5M**
a) Hyper-threading technology b) 64-bit extension technology