Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

IV SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING) MAKE UP EXAMINATIONS, JUNE 2017

ANALOG SYSTEM DESIGN [ELE 2204]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: 21 June 2017** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. Determine v_P, v_N, v_o for the fig Q1A ***(03)***

1B. Design summing amplifier using single opamp to give an output voltage of vo=-5V1+2V2-3V3. Use negetive feedback resistor of 10kΩ ***(03)***

1C. In the figure shown in fig Q1C, assuming negative feedback, determine the resistance (Rin) seen by voltage source. ***(04)***

2A. Design an OPAMP based circuit which converts an input triangular wave having frequencies of range 500Hz to 8Khz into a square wave. Assume C=0.1uf if any. ***(03)***

2B. Discuss the limitations of a Basic Integrator with a neat circuit diagram. How these limitations are overcome in the Practical one? ***(03)***

2C. Design an active wide band reject filter which can reject frequencies from 4kHz to 6Khz with a passband gain of 19db. Gain roll off=20db/decade. Assume C==0.01uf if any. ***(04)***

3A. Realize a suitable Regeneative comparator to obtain V_{UTP}=6V and V_{LTP}=-2V. Assume Vsat=12V, and an input of 20sinwt is applied. Draw the relevant waveforms and VTC. Assume Rf=10k. ***(05)***

3B. What are the conditions to get sustained oscillations? ***(02)***

3C. Design an R-C phase shift oscillator to have fo=2kHz. Assume C=0.1uf if any. ***(03)***

4A. Prove that, frequency of the Opamp square wave generator is independent of Vsat of the OPAMP. ***(03)***

4B. Discuss the working of a Positive Peak detector with a neat circuit diagram. ***(03)***

4C. Design a circuit to generate a wavform shown in fig. 4C, using 555 timer and OPAMPs in linear modes. Doty cycle of the square waveform is 66.6%. Assume C=1uf if any. ***(04)***

5A. Derive the expressions for input and output resistance of a Current series feedback Amplifier ***(04)***

5B. What are the advantages of negative feedback? Justify any two. ***(03)***

5C. Draw the neat circuit of a Sample and Hold circuit and discuss the working. ***(03)***

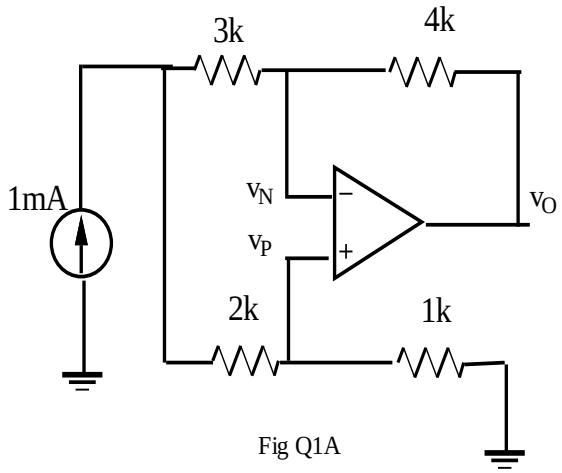

Fig Q1A

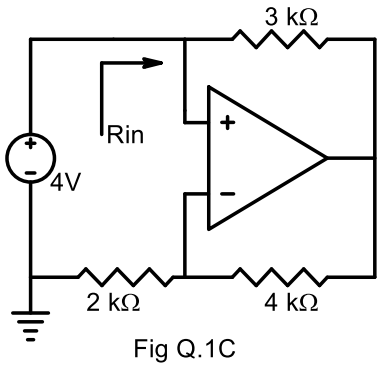

Fig Q.1C

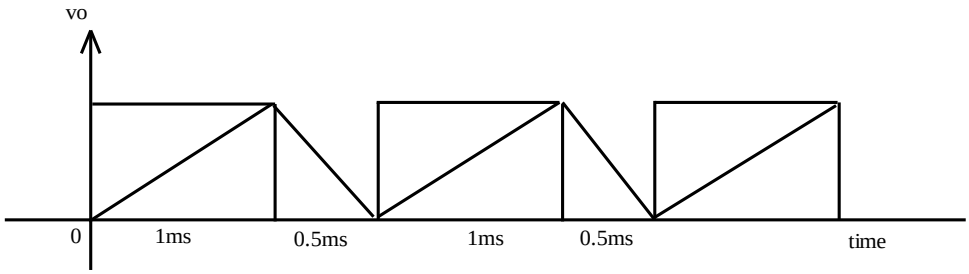

Fig Q 4C