Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY

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A Constituent Institution of Manipal University

IV SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING) END SEMESTER EXAMINATIONS, APRIL - MAY 2017

SUBJECT: DIGITAL SYSTEM DESIGN & COMPUTER ARCHITECTURE [ELE 2203]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: 26 April 2017** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. With example write the difference between

a) continuous assignment statement and procedural assignment statement

b) blocking and nonblocking assignment statement ***(03)***

1B. Write a data flow Verilog HDL code to detect majority of 1's in a 3 bit data input ***(03)***

1C. Write the Verilog HDL code to design a 4 bit binary to gray code converter using 4 to 16 decoder and residual gates, as structural model. ***(04)***

2A. i) Determine the resulting value of Y in the following expression.

```
A: =”10111010”; B: =”100”; C: =”0011”; D: =”110”;
Y: = D + ~ B & C >> 3 ^ A
```

ii) Identify the Synthesized gate for the following program.

```
module ( a, b, y);
Input a, b;
Output y;
always@(*)
if (a)
 if (b)
    begin
 y= 0; else y = 1; end
else if (b)
begin
y = 1; else y= 0; end
endmodule
```

(03)

2B. Write a behavioral Verilog HDL code for an n input OR gate. ***(03)***

2C. Using PLA show how to implement a) full adder b) three input OR gate ***(04)***

3A. Write a behavioral Verilog model for negative edge triggered 2 digit BCD up counter with asynchronous active high reset and synchronous enable. If enable is 1 counter should increment else should stop with current count value. ***(04)***

3B. Draw the Mealy state diagram to detect the following sequences 1001 and 0110, in a continuous data stream (Overlapping is allowed).Hence write the Verilog code for the same. ***(06)***

4A. Consider an expression K = $\frac{R - Q*S}{P + Q/P}$ where P, Q, R, S and K are memory locations. Assuming instructions ADD, SUB, MUL and DIV are available in the instruction set, write an optimized program segments to implement the expression by

i) two address ii) single address and iii) stack based instruction ***(03)***

4B. Perform $120_{(10)}$ x $-30_{(10)}$ using modified Booth's algorithm. Clearly show the contents of all the registers after each iteration. ***(04)***

4C. For a floating point pipeline the segment times are as given below:

T_1=40ns; T_2=230 ns; T_3=180ns; T_4=60ns; T_5 = 50 ns; T_{latch}=20ns;

i) Determine the pipeline clock frequency.

ii) Find the time taken to add 100 pairs of floating point numbers using this pipeline.

iii) What is the efficiency of the pipeline when 200 pairs of floating point numbers are added. ***(03)***

5A. For the state diagram shown in Fig.5A, draw Micro programmed Control Unit and write Micro program. Determine the Size of Control Memory. If hardwired controller is used to develop this state diagram, what is the input of the sequence controller other than clock & reset. ***(04)***

5B. For the 4 level hierarchical memory system shown, if the average access time is 5.29565 ms calculate the access time of level 3.

Level	Access time	Hit ratio
1	150ns	0.45
2	10us	0.71
3	----------	0.80
4	25ms	1.00

(03)

5C. The available space list of a computer memory system is as follows

Starting address	Block Size
100	50
150	200
400	110
600	175

Determine the available space list after allocating the space for the stream of requests consisting of the following block sizes: 100, 25,150

Use a) First fit method. b) Best Fit method. ***(03)***

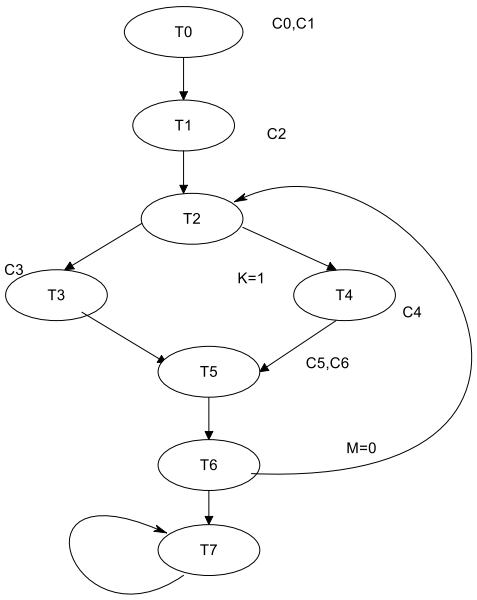

Fig. 5A