Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

IV SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING MAKE UP EXAMINATIONS, JUNE 2017

SUBJECT: DIGITAL SYSTEM DESIGN & COMPUTER ARCHITECTURE [ELE 2203]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: 19 June 2017** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. With example write the difference between **always** statement and **initial** statement ***(02)***

1B. Write a Verilog HDL code to design a 3 bit gray to binary code converter using 4 to 1 multiplexers and residual gates ***(05)***

1C. Consider a function f1 (a,b,c)= ∏M(1,2,4,7) .Show how it can be realized using PLA ***(03)***

2A. Discuss the difference between behavioral model and dataflow model. Illustrate this difference with the help of Verilog HDL code for the Figure Q2A, by writing in both the ways. ***(05)***

2B. Briefly explain the any three datatypes used in Verilog HDL, with examples ***(02)***

2C. Write a short note on Anti-fuse based programming technology ***(03)***

3A. Write behavioral Verilog code for the ASM chart shown in Figure Q3A ***(05)***

3B. Write a Verilog code for JK flip flop. Using this flip fop as an instance, Write a structural Verilog code for a 3 bit UP counter ***(05)***

4A. Which are the dedicated registers of general computer system. What are their tasks? ***(03)***

4B. Perform $-40_{(10)} * 60_{(10)}$ using Modified Booth's algorithm. ***(04)***

4C. With a neat diagram, explain briefly the priority handling concept of Daisy Chain Interrupts. ***(03)***

5A. Given below is the register transfer description of a certain control unit. Draw processing section and the state diagram,

```
Declare registers: A[4],B[4],C[4],D[4],Q[4];
Declare buses : In bus [4] outbus[4];

 Start: A←0100 ,D←0,B← In bus;
        C←In bus, Q←In bus;  /* Content of B,C & Q are Positive */

Loop1:   D←B+C;
          If D=0 go to loop2;
          A←A-1,Q←Q—1,
         If Q<>0 go to loop1;

Loop2:   Outbus←D;

Halt: Go to Halt
```

(04)

5B. Assume a main memory has 4 page frame & assume initially all pages are empty. Consider following stream of page request 1,2,3,4,5,1,2,6,1,2,3,4,5,6,5. Determine the hit ratio for FIFO and LRU replacement policy. ***(02)***

5C. List the different type of mapping technique used between main memory and cache memory? Explain each of them clearly indicating tag field Size ***(04)***

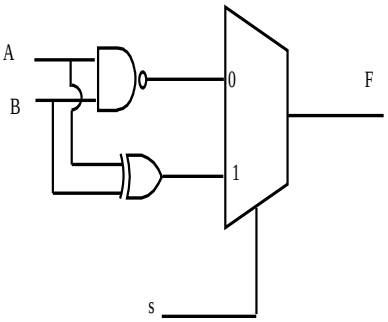

Figure Q2A

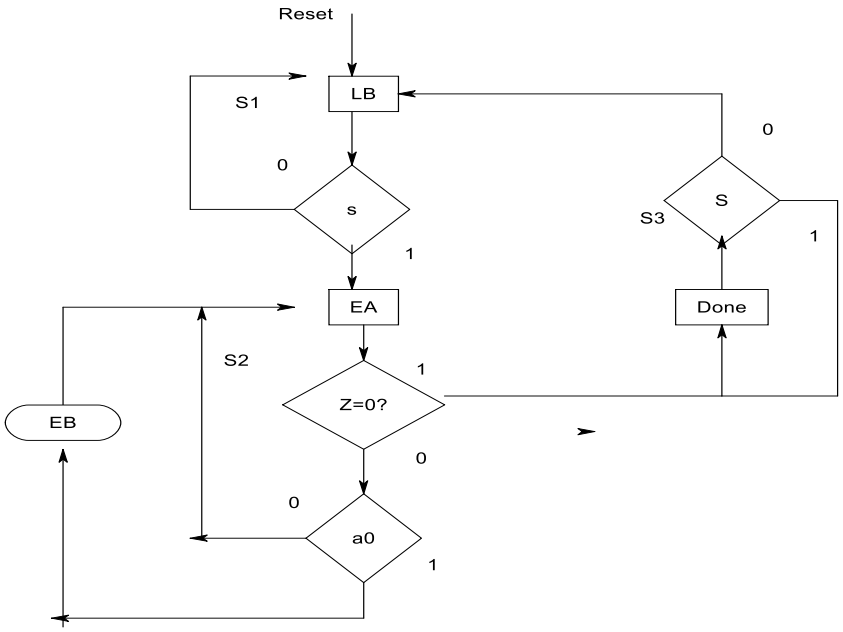

Figure Q3A