Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

FOURTH SEMESTER B.Tech. (E & C) DEGREE END SEMESTER EXAMINATION - April/May 2017

SUBJECT: DIGITAL SYSTEM DESIGN USING VERILOG (ECE-2204)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A.	Implement following functions using Xilinx XC 3000. How many CLBs and LUTs are required? $Y_1 = \bar{x} + y_1$; $Y_2 = x\overline{y_2} + \bar{x}\,\overline{y_1}$; $z = x.y_1$ where Y_1, Y_2 are the next state variables and y_1, y_2 are the present state variables. Here, **x** and **z** are input and output respectively.
1B.	Implement 3-bit Binary-to-Gray code converter using ACT-1 FPGA series. How many minimum number of logic modules are required to implement?
1C.	Explain the Y chart.
	(5+3+2)
2A.	Give the implementation of following function using single ACT3 C logic module. $Y = AB'C'D' + AB'C'E' + AB'C'DE + A'BDE + A'B'C'DE + A'CDE$
2B.	Find the test vector for SA1 fault at node α shown in **FIG. Q2B** using D-Algorithm.
2C.	Write a dataflow Verilog code for 1-bit equality detector.
	(5+3+2)
3A.	Write a dataflow Verilog code for following combinational circuits: [i] N-bit gray to binary code converter [ii] 2-bit equality detector
3B.	Explain scan path technique for testing sequential circuits.
3C.	Find collapse ratio of 3-input NOR gate.
	(5+3+2)
4A.	Find the controllability and observability for the circuit shown in **FIG. Q4A**.
4B.	Find the test vector using path sensitization technique for the circuit shown in **FIG Q4B**
4C.	Find the test vector for SA1 fault using ITG shown in **FIG. Q4C**
	(5+3+2)
5A.	Write a sequential Verilog code for 3-bit ripple up-counter.
5B.	Write switch level Verilog description of 3 input CMOS NOR gate.

5C.	Write a sequential Verilog code for 4-bit parallel adder.
	(5+3+2)

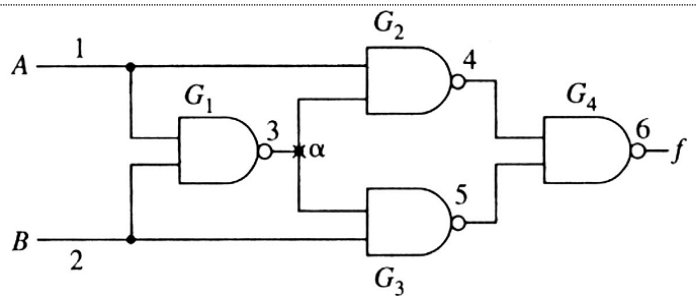

FIG. Q2B

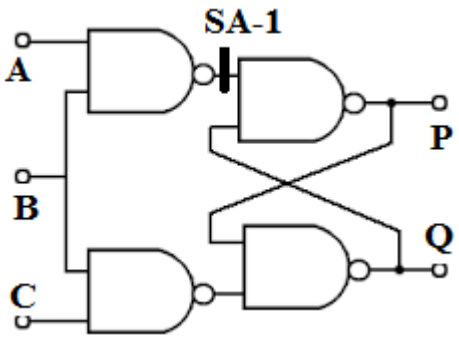

FIG. Q4C

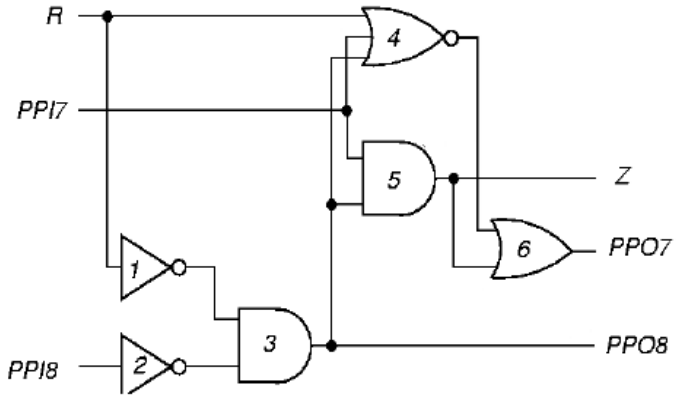

FIG. Q4A

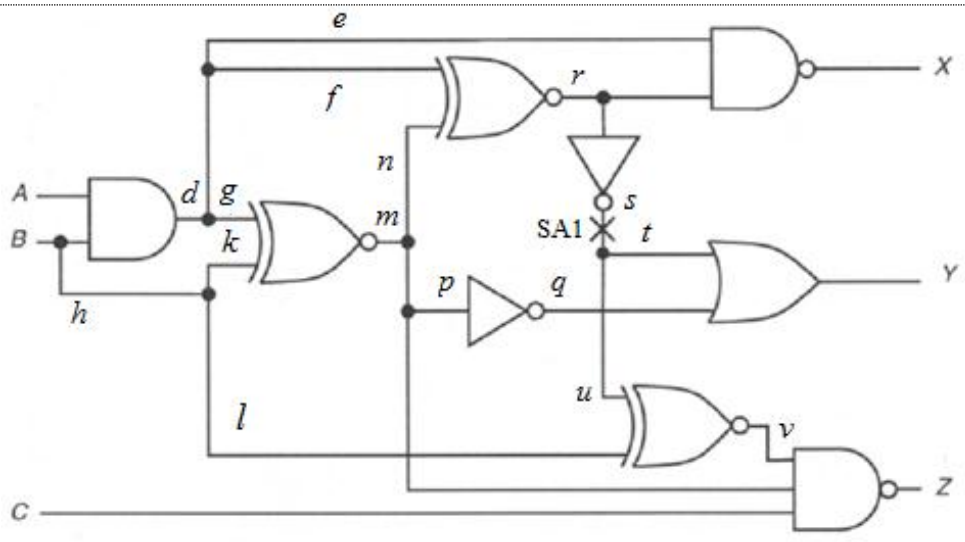

FIG. Q4B