Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

FOURTH SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION – APRIL / MAY 2017

SUBJECT: DIGITAL SYSTEM DESIGN USING VERILOG (ECE-2204)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. [i] Implement the below given logic function using single ACT2 C logic module.

$$Z = A'B'C'E + A'B'D'E + A'B'CDF' + ACD + BCD$$

[ii] Implement following function using Xilinx XC 3000. How many CLBs and LUTs are required?

$$F(a, b, c, d, e) = a.b.c + a.\bar{b}.c + \bar{e} + d.e$$

1B. Explain the ASIC design flow.

1C. Compare ACTEL and XILINX FPGA with respect to following: [i] logic cell [ii] reprogrammability [iii] switching element.

(5+3+2)

2A. Find TV to test SA0 fault for the circuit shown in **FIG. Q2A** using D algorithm. Show all the steps showing cubes used and their cube intersection.

2B. Implement the following expression using PAL (Altera MAX FPGA) architecture having 3 wide OR array. $F = \bar{A}\,CD + \bar{B}\,CD + AB + B\bar{C}$

2C. Write structural Verilog code to model two-input XOR gate using basic gates.

(5+3+2)

3A. Write structural Verilog code for 4 bit SIPO/ PISO shift register.

3B. Find TV to test SA1 fault for the circuit shown in **FIG. Q3B** using PODEM algorithm.

3C. Explain the syntax of any one conditional sequential statement used in Verilog.

(5+3+2)

4A. [i] Find the controllability and observability measures of all the nodes for the circuit shown in **FIG. Q4A** using SCOAP method.
[ii] How would you reduce test generation cost in testing large counters?

4B. Write a structural Verilog code for full-adder with half-adder as component. Model the half-adder component using a data-flow model.

4C. Write a dataflow Verilog code for N-bit magnitude comparator.

(5+3+2)

5A. [i] Find the test vector for sequential circuit shown in **FIG. Q5A** using ITG.

[ii] State the merit and demerit of Boolean difference (BD) testing method.

5B. Write a Behavioral Verilog code for 8:3 encoder.

5C. Write a Behavioural Verilog model for 4-to-1 multiplexer using case statement.

(5+3+2)

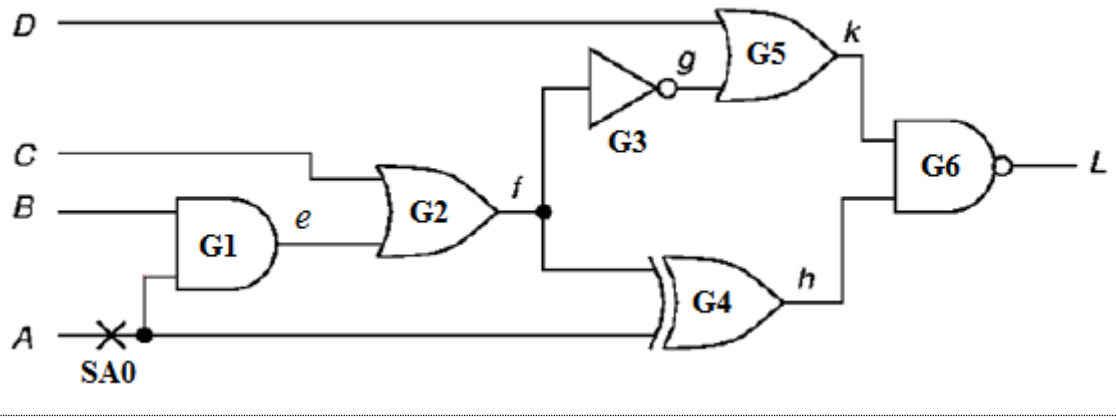

FIG. Q2A

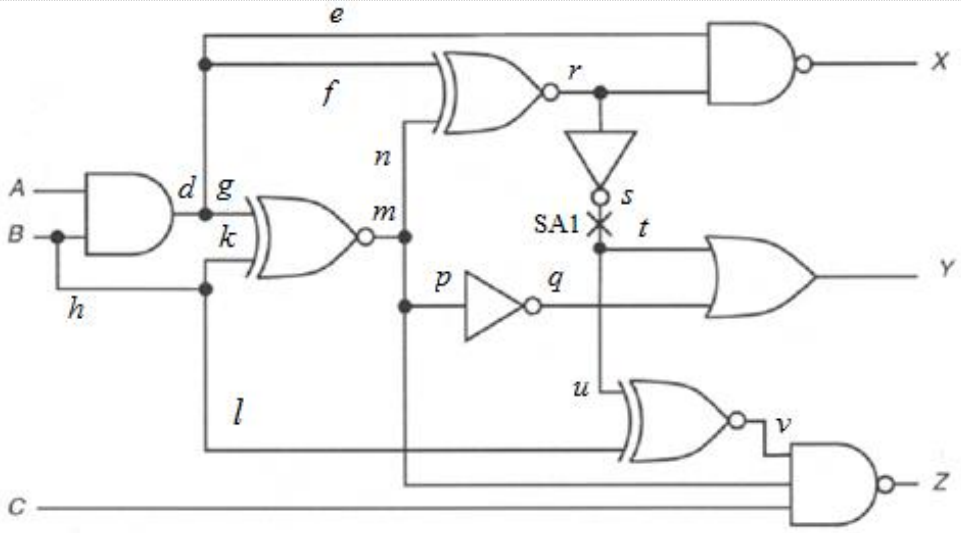

FIG. Q3B

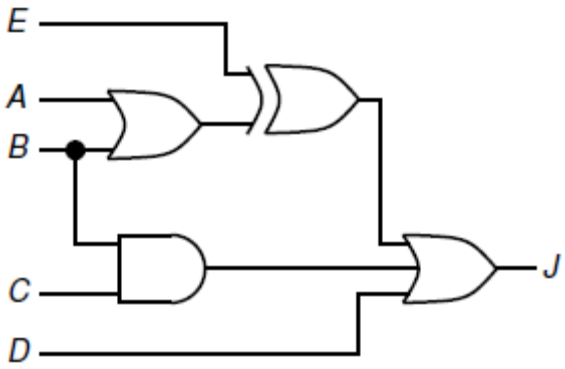

FIG. Q4A

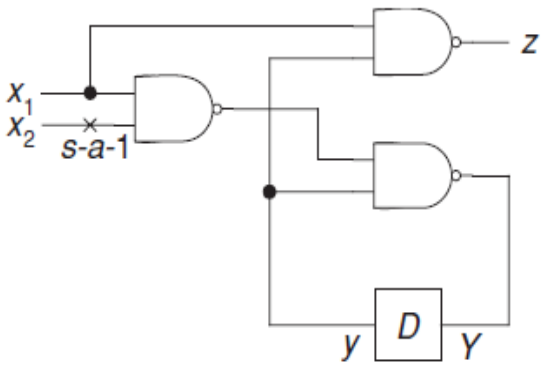

FIG. Q5A