Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

FOURTH SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION - APRIL / MAY 2017

SUBJECT: ELECTRONIC PRODUCT DESIGNAND PACKAGING (ECE - 3282)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Explain the importance of Aesthetics and Ergonomic in industrial design?

1B. Explain with neat diagram product life cycle?

1C. Explain in few words any four print finishing techniques?

(5+3+2)

2A. What is a heat sink? Explain with diagrams the thermal circuit with and without heat sink?

2B. What is product detailing? Explain any two product detailing techniques?

2C. Draw a neat diagram of failure rate cure and explain?

(5+3+2)

3A. Explain the chip making process with neat block diagram?

3B. List and explain the factors to be considered while designing heat sinks?

3C. In a given CMOS IC system the load capacitance is 0.4fF, the operating voltage is 1.5V, the operating frequency is 2.80 GHz and the number of transistors used in the system is 55,000,000. What is the power consumed by the system?

(5+3+2)

4A. What is wire bonding? Explain with neat diagram two wire bonding techniques?

4B. Explain with neat diagrams different types of level one packaging?

4C. How ground and supply noise is generated? What are the remedial measures?

(5+3+2)

5A. Explain the grounding and shielding noise reduction techniques?

5B. Discuss reflection and crosstalk noise with necessary diagrams?

5C. With neat diagram explain noise path?

(5+3+2)