Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

FOURTH SEMESTER B.Tech. (E & C) DEGREE END SEMESTER EXAMINATION
May 2017
SUBJECT: I C Systems (ECE - 2202)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1(a)	Derive the transfer characteristics for an emitter coupled differential amplifier using BJT and highlight the salient information that can be read from the graph.
(b)	For the circuit shown in Fig.Q.No.1.b., determine the collector currents through transistors Q1 and Q2, and calculate the value of resistance Rc required to obtain Vo=6V. Assume β=200.
(c)	Why level shifters are needed in op-amps? Give reasons. Explain the operation of at least one level shifter circuit. (5+3+2)
2(a)	For the circuit shown in fig. q.no.2.a, determine the output voltage Vo.
(b)	Design a practical differentiator circuit that can differentiate a max frequency of 5kHz. and draw the output wave form for a square wave input of 200Hz with 2V peak to peak.
(c)	Draw the circuit of a V-I converter with floating load and show that the current is independent of load. (5+3+2)
3(a)	Draw the circuit of an instrumentation amplifier using three op-amp and derive the expression for the gain.
(b)	It is required to band limit voice signal to 4kHz., before applying for further processing to avoid aliasing. The rate of attenuation in the transition band should be at least 60dB/decade and pass band gain of 8. Design appropriate Butterworth filter.
(c)	Derive the transfer function of the circuit shown in fig.q.no.3.c. and indicate the function performed by the circuit. (4+3+3)
4(a)	Design a circuit using 555 Timer to generate a free running pulse train of 5kHz. with 50% duty cycle and peak amplitude 10Volts. Derive the expressions used.
(b)	With the help of a neat block diagram, explain how the input frequency can be multiplied by a factor of 4 using PLL.
(c)	Explain the terms i) Capture range and ii) Lock in range as applicable to PLL. Also state the name of the functional block of PLL that controls each of the above parameters. (4+3+3)
5(a)	With help of a neat diagram explain the operation of flash ADC which converts the given analog input into equivalent three bit binary code. List the salient features of the circuit.
(b)	With help of a neat diagram explain the operation of dual slope ADC.

(c)	If in an 12-bit DAC, the reference voltage used is +12V, calculate i) the resolution ii) The full scale output voltage and iii) the output voltage corresponding to the binary input of 101011001100
(d)	Design a circuit to generate a time delay of 20msec on demand, using 555 Timer. (2.5 X 4 =10)

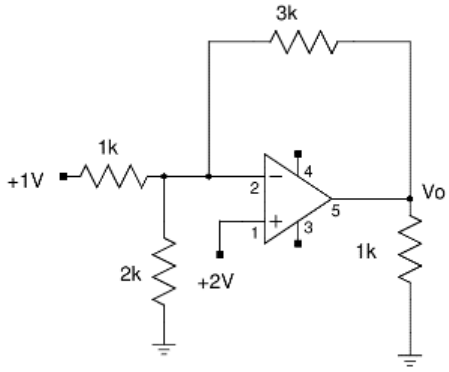

Fig.Q.No.2.a

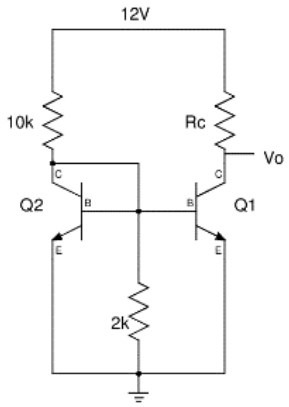

Fig.Q.No.1.b.

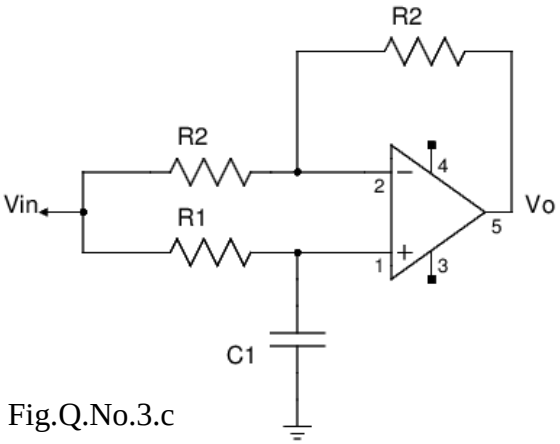

Fig.Q.No.3.c