Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

FOURTH SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION
APRIL / MAY 2017
SUBJECT: IC Systems (ECE - 2202)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. For the circuit shown in Fig Q1A, determine i) DC voltages at nodes V_1,V_2, and V_3. ii) CMRR and iii)Differential gain. Assume $I_s = 10^{-16}$ A and $V_A = 10$ V.

1B. Why current mirrors are used in differential amplifiers? Explain and design a current mirror circuit using BJTs to provide a current of 10mA. Assume a Vcc of 10 Volts and $V_{BE} = 0.65$V. Draw the circuit diagram.

1C. Design a level shifter circuit using active load to shift the voltage level from 2V to 0.2V. Assume V_{CC}=3V, V_{EE} = -3V, $I_s = 10^{-16}$ A and I_{ref}=2mA.

(5+3+2)

2A. For the circuit shown in Fig.Q2A, determine the output voltage Vo. Assume ideal op-amps.

2B. For the circuit shown in Fig.Q2B, if V_{in}=1V, determine the following: i) V_o if CMRR= 100 dB ii) V_{out} if there exists 1% mismatch between two resistors R_1 iii) V_o if there exists 1% mismatch between two resistors R_2 .

2C. It is required to amplify a square wave with 1V peak to peak by a factor of 3 using an op-amp circuit with rise time at the output not be more than 4μsec. Calculate the minimum slew rate required for the op-amp. (5+3+2)

3A. Temperature sensor installed in a room generates DC voltage in the range 0 to 4V proportional to a variation of temperature from 0^0C to 40^0C. The air-conditioner should be turned on whenever the temperature goes above 25^0C and to be turned off whenever it goes below 20^0C. Design a suitable circuit to generate switching waveform making excursion between 0 and 5Volts to control the air conditioner using a single op-amp. Derive the expressions used.

3B. Design a Butterworth active band elimination filter to reject frequencies in the range of 1kHz to 10kHz. The circuit must provide a pass band gain of 6 and roll off rate in transition bands is 40dB/decade.

3C. What are the key merits and demerits of active filters? (5+3+2)

4A. Design a circuit using 555 timer to divide the frequency of an input pulse train of 5kHz by a factor of 5. The peak amplitude of the output required is 10 Volts. Assume C=0.1µF. Derive the expression used.

4B. With the help of a neat block diagram explain the operation of PLL and define key parameters.

4C. With the help of a neat block diagram, show how frequency translation can be implemented using PLL.

(5+3+2)

5A. If in a 4 bit DAC designed using R-2R ladder network with Vref =5V, calculate the value of output analog voltage, if the binary input data is 1000 using appropriate analysis.

5B. With the help of a neat diagram, explain the operation of Successive Approximation Register (SAR) type of ADC. List the salient features of this ADC.

5C. A dual slope ADC uses an 18-bit counter with 5MHz. clock. The maximum input voltage is +12V and the maximum output of an integrator, when the counter completes one round of counting (2^{18}), is -10V. If R=200kΩ, determine i) the value of the capacitance required. ii) the decimal equivalent value of digital data displayed, assuming V_{ref}= -10V for an input of 5.237V. iii) conversion time for the above case.

5D. Design a Schmitt trigger circuit using 555 timer to get UTP=8V, LTP=4V and output peak voltage is 10V. Suggest modifications to the circuit if UTP and LTP need to be changed dynamically.

(2.5 x 4 =10)

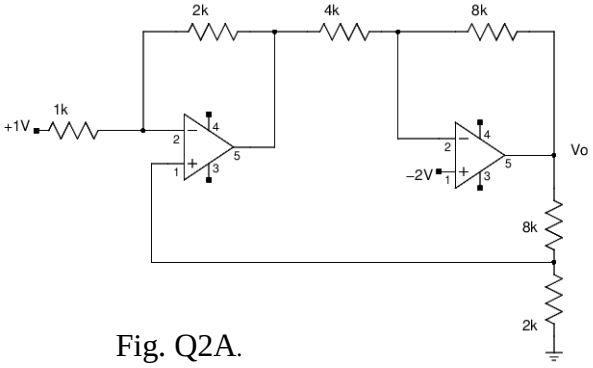

Fig. Q2A.

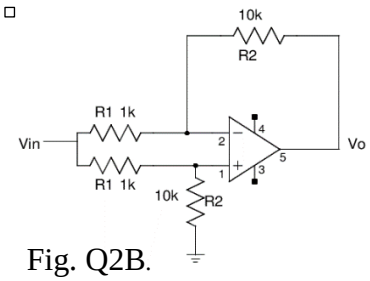

Fig. Q2B.

Fig. Q1A.