Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

FOURTH SEMESTER B.TECH. (INSTRUMENTATION AND CONTROL ENGG.)

END SEMESTER EXAMINATIONS, APRIL/MAY 2017

SUBJECT: ANALOG SYSTEM DESIGN [ICE 2204]

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A.	Obtain the expression for V_o in the circuit shown in Fig. Q1A.	**3**
1B.	Draw the block diagram of an op-amp. Explain the function of each block.	**3**
1C.	Explain the working of differential amplifier circuit using transistors in common mode.	**4**
2A.	Draw the circuit diagram of the differential instrumentation amplifier using a transducer bridge. Derive the expression for V_o.	**3**
2B.	For the double integrator circuit shown in Fig. Q2B, prove that the transfer function is given by the following expression. Assume that the op-amp is ideal. $$\frac{Vo(s)}{Vi(s)} = \frac{1}{(RCs)^2}$$	**3**
2C.	Derive the expression for the transfer function of a 2nd order high pass butterworth filter.	**4**
3A.	With relevant circuit diagram and waveforms, derive the expression for frequency of oscillations of astable multivibrator using op-amp.	**5**
3B.	Describe the working of monostable multivibrator using 555 timer with internal block diagram and output waveforms. Derive the expression for pulse width.	**5**
4A.	Derive the expression for frequency of RC phase shift oscillator with relevant circuit diagram.	**4**
4B.	Explain the working of Voltage Controlled Oscillator with internal block diagram and output waveforms. Also derive the expression for its frequency of oscillation.	**4**
4C.	Design Wien bridge oscillator with f_o = 1.5KHz. Assume C = 0.01µF.	**2**
5A.	Explain Successive Approximation ADC. For a 4 bit Successive Approximation ADC with an analog input of 11.3V, determine the output at each clock cycle.	**5**
5B.	Design a 4 bit weighted-resistor DAC whose full scale output voltage is -5V. The logic levels are 1 = +5V and 0 = 0V. What is the output voltage when the input is 1101? Assume R_f = 10KΩ.	**3**
5C.	Define Resolution and Settling time for a DAC	**2**

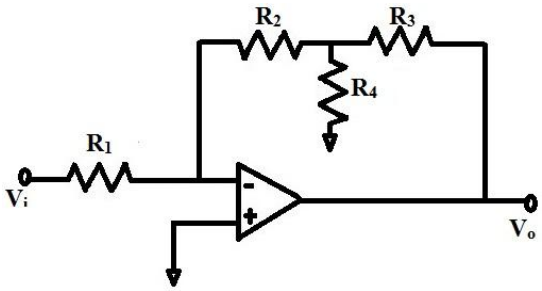

Fig. Q1A

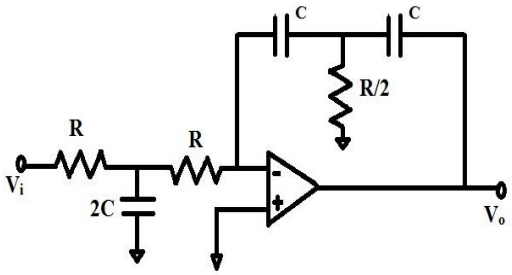

Fig. Q2B

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