Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

II SEMESTER M.TECH. (COMPUTER SCIENCE & ENGINEERING)

END SEMESTER EXAMINATIONS, APRIL/MAY 2017

SUBJECT: COMPILERS & ADVANCED OPERATING SYSTEMS

[CSE 5201]

REVISED CREDIT SYSTEM
(20/4/2017)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitable assumed.

1A. Draw transition diagram for accepting unsigned numbers. The number may consist of many digits and may be an integer or a real number. The real number may be expressed in decimal or exponential notation. Show how it accepts integers and real numbers with an example for each. **5M**

1B. Consider the grammar
S → A | L
A → digit | id
L → (K) **5M**
K → S,K | S
Left factor this grammar. Construct First and Follow sets for the non-terminals of the resulting grammar. Also, construct LL (1) parsing table.

2A. Construct LR(0) DFA for the given grammar.
A → SA | a **5M**
S → AS | b

2B. Construct LR(1) DFA for the following grammar. Also construct the Canonical LR parsing table **5M**
A → (A) | a

3A. Given the grammar T → FT'
T' →*FT' | ε
F → digit **4M**
Write the semantic rules for evaluation of expressions like x*y. Also write the annotated parse tree for the expression 2*3*7.

3B. Given the expression "a + (b - c) * a + d * (b - c)". Write the DAG, three address code and the equivalent triple representation. **4M**

3C. List the issues encountered in the design of a code generator. Explain any two of them. **2M**

4A. With a diagram, explain the implementation of RMI. Also, explain the role of the different modules. **5M**

4B. Explain Lamport's algorithm for synchronizing logical clocks. Illustrate with an example. **5M**

5A. With reference to a multiprocessor system, explain the different atomic hardware instructions used to implement the lock operation during process synchronization. **5M**

5B. What are the main features of the ARM Architecture? Also explain about the ARM registers, Exceptions and Status registers. **5M**

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