Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
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SECOND SEMESTER M.TECH (DEAC & ME) DEGREE END SEMESTER EXAMINATION - APRIL / MAY 2017
SUBJECT: SYSTEM ON CHIP DESIGN (ECE - 5256)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Define co-synthesis in system level design flow. Discuss the fundamental design problems those need to be addressed by the co-synthesis.

1B. Write the characteristics that Digital Signal Processor should have over general purpose processor.

1C. Draw a neat diagram of ASIC design flow

(5+3+2)

2A. Design a coin operated public telephone unit based on FSM model for the following requirements.
A. The calling process is initiated by lifting the receiver (off-hook) of the telephone unit.
B. After lifting the phone the user needs to insert a 1 rupee coin to make the call.
C. If the line is busy, the coin is returned on placing the receiver back on the hook (on-hook).
D. If the line is through, the user is allowed to talk till 60 seconds and at the end of 45^{th} second, prompt for inserting another 1 rupee coin for continuing the call is initiated.
E. If the user doesn't insert another 1 rupee coin, the call is terminated on completing the 60 seconds time slot.
F. The system is ready to accept new call request when the receiver is placed back on the hook (on-hook).
G. The system goes to the 'Out of Order' state when there is a line fault.

2B. Write the differences among the following
i. Hard processor and soft processor
ii. Zynq SoC and Discrete FPGA-Processor combination
iii. Multitasking and Multiprocessing

2C. With example, explain the dynamic reconfiguration of PSoC.

(5+3+2)

3A. Explain the ways ARM Instruction set differs from pure RISC definition so that it suitable for embedded applications.

3B. What is AMBA? Draw typical AMBA based system and explain its associated buses.

3C. In ARM memory system, Draw the ROM wait control state transition diagram and explain the reason of introducing wait states while accessing ROM.

(5+3+2)

4A. Write static voltage scaling algorithm for EDF and RM schedulers. Implement the same for the task set given in **Table 4.1.** For each scheduler, find the minimum frequency to which the task set can be scaled down and draw the scheduling graph.

Task	Computing time	period
1	3ms	8ms
2	3ms	10ms
3	1ms	14ms

Table 4.1

4B. Three processes with execution times as shown in Table 4.2 enter the ready queue in the order P3, P1, P2.
i. calculate their turnaround time for the FIFO algorithm.
ii. If they choose to use the round-robin scheme with a slice time of 10 units, how will the scheduling change? Show with appropriate graphs.

Table 4.2

Process No	Execution time
P1	40
P2	55
P3	25

4C. In non-OS based embedded software implementation, write the procedures to process I/O request once an interrupt arises.

(5+3+2)

5A. i. What is the difference between synchronous and asynchronous exceptions? Explain with example.
ii. What is exception frame and explain its necessity.
iii. Write difference between exception service routine and interrupt service routine

5B. Write low energy I/O device scheduling algorithm for two state I/O devices

5C. Explain the way how the following approaches help in lowering the operating voltage of SoC without sacrificing the performance of the system.
i. Multiple voltage assignment
ii. Dynamic voltage scaling

(5+3+2)